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A 128 K-BIT
CCD BUFFER MEMORY SYSTEM

By
K.H. Siemens
R.W. Wallace
C.R. Robinson

July 1976

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Prepared under Contract NAS1-13507

By

BELL-NORTHERN RESEARCH LTD.

Ottawa, Ontario, Canada

for

NASA

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FOREWORD

This final report was prepared by Bell-Northern Research, Ottawa, Ontario, Canada, for NASA's Langley Research Center under NASA Contract No. NAS1-13507. It describes work performed from August 20, 1974 to February 6, 1976, in the LSI Device Applications Group of the Silicon Technology Laboratory. The project supervisor is Mr. C. R. Robinson. Dr. K. H. Siemens and Mr. R. W. Wallace participated in the development of the memory system and the custom memory exerciser. Dr. S. D. Rosenbaum, Mr. D. E. Brown and Mr. J. T. Caves also participated in the initial design phase or assisted in the debugging of the memory system. The NASA Project Monitor is Mr. A. Fripp.

Development of the 8K CCD memory devices which were used in the memory system was begun prior to the start of this contract. Some characterization of these devices was carried out in a parallel research program, funded by BNR, during the course of the contract. While 87% of the effort described in this report has been funded by NASA Langley Research Center, the remaining 13% was supported by Bell-Northern Research.

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ABSTRACT

A prototype system has been implemented to demonstrate that CCD's can be applied advantageously to the problem of low power digital storage and particularly to the problem of interfacing widely varying data rates. 8K-bit CCD shift register memories were used to construct a feasibility model 128K-bit buffer memory system. Serial data that can have rates between 150 KHz and 4.0 MHz can be stored in 4K-bit, randomly-accessible memory blocks. Peak power dissipation during a data transfer is less than 7 W., while idle power is approximately 5.4 W. The system features automatic data input synchronization with the recirculating CCD memory block start address. This report provides descriptions both of the buffer memory system and a custom tester that was used to exercise the memory. The testing procedures and testing results are discussed. Suggestions are provided for further development with regards to the utilization of advanced versions of CCD memory devices to both simplified and expanded memory system applications.

A 128 K-BIT CCD BUFFER MEMORY SYSTEM

By K. H. Siemens, R. W. Wallace, and C. R. Robinson
Bell-Northern Research

SUMMARY

A prototype system has been implemented to demonstrate that CCD's can be applied advantageously to the problem of low power digital storage and particularly to the problem of interfacing widely varying data rates. Mass or "bulk" data storage is presently generally configured in serial form and usually comprises magnetic media, namely disc or tape. Each of these place limitations in terms of access speed, data bandwidth capability, and power, these systems being electromechanical in operation. Magnetic bubble memory overcomes the latter objection but still presents bandwidth and access speed limitations. Therefore, any consideration of CCD's as a memory medium must take into account the total system objectives. It is feasible to consider a bulk memory consisting either totally of CCD memory or alternately consisting of a combination of two media, such as CCD and magnetic bubble, or CCD and RAM, to combine speed with low power as in the system herein described. The present study and prototype system is centered around relatively long term storage of sequentially arriving data, in fact a data recorder.

CCD memories each containing 32 shift registers with a length of 256 bits have been arranged to form 32 independently accessible memory blocks. Each memory block has the capacity to store 4096 serial input data bits on a first-in, first-out basis. The system is capable of handling both input and output data rates from less than 150 KHz to greater than 4 MHz. Any length of data input stream, from 1 bit to the full memory capacity of 128 K-bits, can be stored during a transfer operation. Peak power dissipation during a data transfer at the maximum data rate is less than 7W. Idle power is approximately 5.4 W. The memory system was thoroughly exercised with a custom memory tester to determine the operating characteristics.

A considerable amount of logic has been included in this prototype unit to facilitate manual control. With further system optimization and computer control, it is expected that the idle power could be reduced to less than 2 watts, with a corresponding decrease in peak power dissipation. The system capacity could be expanded with relative ease either by increasing the number of memory blocks in a modular fashion or by providing for parallel data storage. The power dissipation does not increase proportionally to memory capacity since a major portion of the power is consumed in the peripheral logic which does not expand significantly with increased memory capacity. A discussion of alternative system architectures built around more advanced device configurations concludes this report.

I. INTRODUCTION

The 128 K-bit CCD buffer memory system that is described in this report was developed at Bell-Northern Research to demonstrate the feasibility of using charge coupled digital memory devices in a system configuration suitable for buffering or storing data occupying a wide bandwidth. After an engineering design study was performed, a buffer memory system incorporating the Bell-Northern Research 8 K-bit CCD was fabricated as a feasibility model. The system is organized as 32 independently-accessible blocks, each having a capacity of 4096 (4K) bits. It has been demonstrated that the memory system can accept, store, and read out serial data streams of any length up to full memory capacity and with transfer rates from 150 KHz to 4.0 MHz.

Although the memory is indeed a low power system, it still contains considerable circuitry that is included primarily to facilitate manual control. Thus the system has not yet been fully optimized for low power operation since much of the circuitry could either be removed if computer control was available or replaced by CMOS logic in single gate or custom LSI form. However, peak system power at the maximum transfer rate is less than 7 watts, whereas idle power is close to 5.4 watts because of the particular circuit implementation used.

The report discusses the controls, I/O signals, and the operational capabilities of the demonstration system. System specifications are provided. A detailed description of the memory system is followed by a description of the tester that was built to exercise the buffer memory. An outline of the tests that were performed and their results is given. System limitations and areas for improvement and further development of CCD systems are discussed.

II. SYSTEM CHARACTERISTICS

2.0 Introduction

This section is intended to provide a general understanding of the memory system and its operation. System specifications are given. Features of the internal memory structure, panel controls and indicators, and system operation from an external point of view are provided.

2.1 System Specifications

The memory system meets the following specifications:

a) Power supplies -

$$V_{CC} = 5 \text{ VDC} \pm 5\% @ 2 \text{ amps.}$$

$$V_{DD} = 10 \text{ VDC} \pm 2\% @ 1 \text{ amp.}$$

$$V_{BB} = -3 \text{ VDC} \pm 5\% @ 50 \text{ mamps.}$$

The current limits are those recommended for the power supplies.

They do not refer to actual memory system current drain. V_{DD} and V_{BB} are nominal operating points recommended for low power operation. Further explanation of the operating range is made later.

b) Power Consumption -

Read/Write operation < 7 watts

Idle operation < 5.5 watts

c) Memory Capacity -

Capacity = 128 K bits (K = 1024)

Memory block size = 4 K bits

No. of blocks = 32 (individually accessible)

d) Clock Input -

TTL compatible clock with frequency 150 KHz to 4.0 MHz.

Minimum clock pulse width = 35 nsec.

e) Data Input -

TTL compatible, non-return-to-zero (NRZ) data synchronized with rising edge of clock input. Presence of valid data input is determined by a LOW-true signal (Data Input Available) that is synchronized with the data. One channel for serial data input is provided.

f) Data Output -

TTL compatible, NRZ data output is synchronized with the rising edge of the input clock. Valid data output is presented serially on one channel in synchronism with a LOW-true Data Output Available signal. Data is read-out on a first in-first out basis for each block.

g) Access Frequency -

Both WRITE and READ frequencies are determined by the input clock rate, 150 KHz to 4.0 MHz.

h) Idle Frequency -

Idle frequency is maintained at less than 20 KHz provided the input clock is maintained at frequencies between 150 KHz and 4.0 MHz.

i) Operating Temperature -

The system may be operated at normal room temperatures without special environmental controls.

2.2 Memory Structure

The memory system has the capacity to store 128K data bits in 32 separate memory blocks of 4 K bits each. 8K CCD's developed at Bell-Northern Research are used as the storage medium. Complete specifications of CC8M03 CCD decoded memory chip are given in Appendix A. Appendix B contains a paper which provides further detail on the chip design and device characteristics. These devices contain 32 dynamic, recirculating

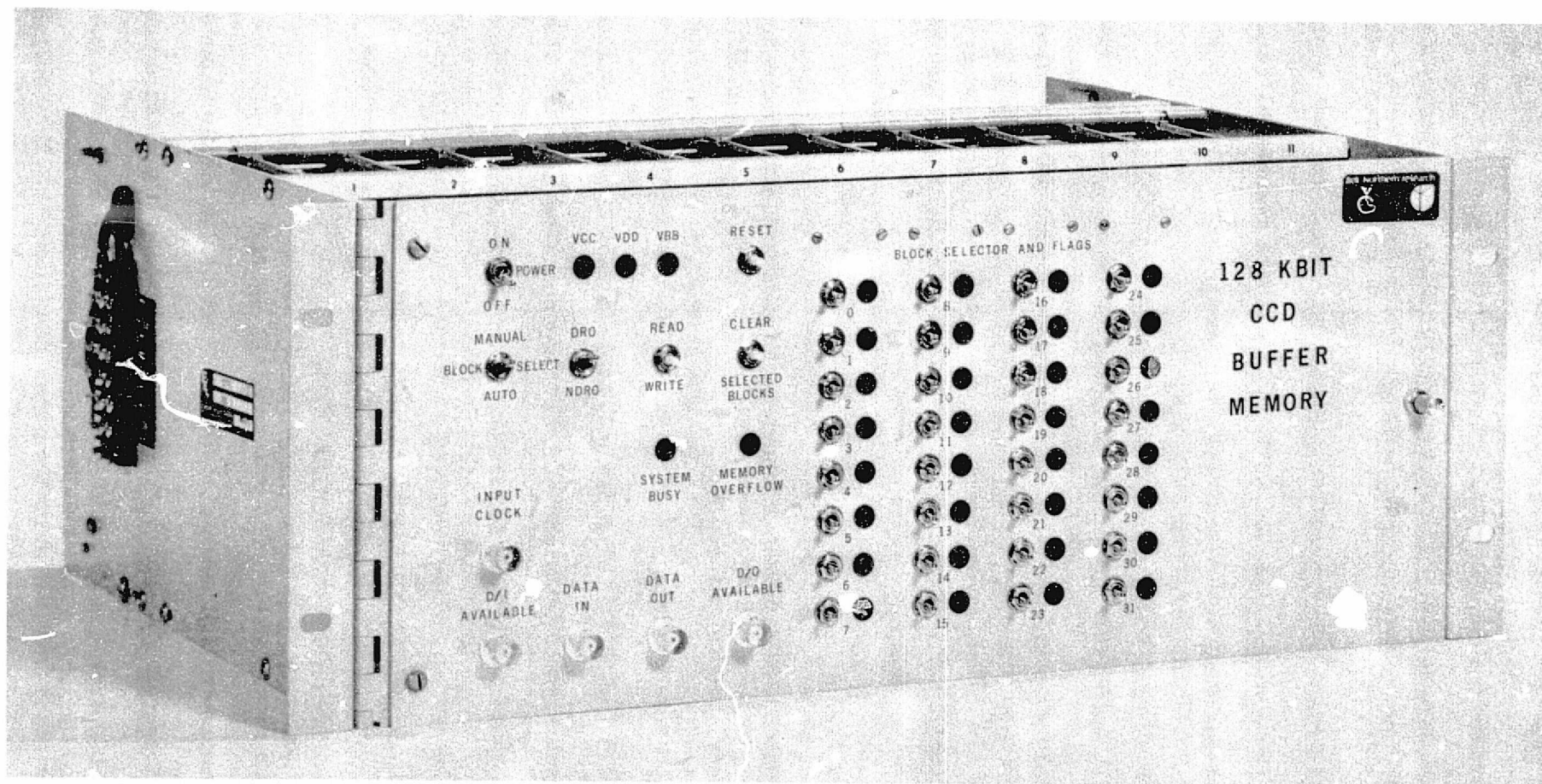


Fig. 2-1 Memory System Front Panel

shift registers of tracks, each of length 256. Since 4-way multiplexing of the serial input data streams was required to achieve high data transfer rates, the CCD's are arranged in 4 banks of 4 devices each. Hence, each bank of CCD's can store 8 memory blocks.

During a data transfer, all 4 CCD's in the accessed bank are clocked at the access rate (i.e., $\frac{1}{4}$ data rate), while the rest of the memory devices in the system operate at $\frac{1}{4}$ the access rate in order to maintain address synchronization at the end of each memory block transfer. Details of addressing and data location synchronization are provided in a later section. Random access to any memory block or ordered set of blocks is permitted.

2.3 Panel Controls and Indicators

Before the memory system operating modes are discussed, an outline of front and back panel controls, I/O signals, and indicators is given. Reference may be made to Figure 2-1 which shows a photograph of the memory system front panel. It should be kept in mind that many of the controls are provided only to facilitate manual control of this prototype system. They are not required for a system under computer control.

a) Power supplies -

Three power supplies are required, V_{CC} , V_{DD} , and V_{BB} , with nominal voltages as given in the system specifications. In order to study system operating ranges and power consumption, the V_{DD} and V_{BB} supplies may be varied safely within the following limits:

$$+8V_{DC} \leq V_{DD} \leq 14 V_{DC}$$

$$-7V_{DC} \leq V_{BB} \leq -1 V_{DC}$$

Power supply connections can be made either on the back panel or on the left side of the cabinet. A power supply switch and 3 LED indicators to monitor each supply are provided on the front panel.

b) Reset -

A pushbutton reset control is provided to initialize logic in the memory system. This button should always be pressed after power turn-on and the input clock is running.

c) Block selectors and block flags -

32 sets of switches and LED indicators are provided to control access to the memory blocks. The switches and LED's are arranged to correspond to the 8 memory blocks in each of the 4 banks of CCD's. The switches are used to select a memory block for a data transfer and the LED's indicate the status of the block-in-use flags; where ON indicates block-in-use, and OFF indicates a block available for storage.

d) Manual/Auto Select -

This toggle switch is used to enable the block selector switches when in manual mode. Only those blocks selected by the block selector switches will be written into or read. In auto mode the block selector switches are over-ridden and all empty blocks are available to accept input data in WRITE mode; all blocks containing data are read in READ mode.

e) READ/WRITE Select -

The system is normally set up to accept input data at any time, i.e., continuous WRITE mode. The READ/WRITE select pushbutton is pressed to start a memory READ operation.

f) NDRO/DRO Select -

Two types of readout operations are permitted. Non-destructive readout (NDRO) permits a memory block to be accessed without disturbing either the data contained in the memory or the status of its corresponding block-in-use flag. Destructive

readout (DRO) causes the block-in-use flag to be reset after a READ transfer request, thereby making the block available to accept new data. Data within the CCD normally recirculates on each track and is destroyed only by overwriting or stopping the transfer clocks for a period greater than the maximum refresh interval.

g) Clear Selected Blocks -

Pressing this button clears all block-in-use flags of those blocks selected by the block selector switches.

h) System Busy Indicator -

An LED is on for the duration of a WRITE or READ transfer operation.

i) Memory Overflow Indicator -

An LED indicates the availability of blocks to accept new data.

The indicator will be on during idle or WRITE mode either when all blocks are used in AUTO mode, or all selected blocks are used in MANUAL mode. The LED will be off during a READ transfer.

j) I/O Connectors -

Five standard BNC connectors are provided on the front panel for input/output signal connections. All I/O signals are TTL compatible.

An input clock is used to drive the memory system. The clock must be available at all times within a frequency range of 150 KHz to 4.0 MHz. Input data should be NRZ and synchronized with the input clock. Availability of valid data is to be indicated by a LOW-true signal, also synchronized with the input clock.

Output data and a data output available signal are provided with the same specifications.

k) BA Connector Socket -

This rear-panel socket is used to provide the block address signals both of the next block to be accessed and the block currently

being accessed. The signals may be used for testing, monitoring, or control.

l) VAS Connector Socket -

Similar to the BA socket, various timing signals (to be described later) are made available.

m) TPA Connector -

This edge connector, mounted on the rear panel, is used to facilitate access to a number of test points within the system. Schematics for all front and back panel connectors, controls, and indicators are shown on sheet 16 of Appendix C.

2.4 System Operation

The system operation involves 4 main phases,

- (1) start-up procedure,
- (2) WRITE operation,
- (3) system idle,

and (4) READ operation.

(1) Start-up of the system involves presetting the power supplies V_{DD} , V_{CC} , and V_{BB} . A single power-on switch activates all the supplies. A TTL-level clock with frequency in the range 150 KHz to 4.0 MHz is to be provided. The reset switch must be pressed to initialize the system logic.

(2) The memory system can accept for storage in a WRITE operation any serial data stream that is synchronized with the input clock. Valid data is recognized by the presence of a second, coincident, LOW-true signal at the system "data input available" connector. Since data is synchronized with the input clock, data rates from 150 KHz to 4.0 MHz can be accepted. Data burst lengths from 1 bit to the amount of available memory locations can be stored.

Before a WRITE operation begins, memory storage locations should be selected. In AUTO mode, all empty memory blocks are available, with the first portion of the data stream - up to 4K data bits - being stored in the first available block. If the data burst length exceeds 4K bits, memory locations in the next empty block are used. Thus, all empty blocks comprise an ordered set of available memory locations. If less than a block length of data is written, the remainder of the accessed block is filled with non-valid data. The WRITE sequence ends automatically at the end of a block transfer when no further input data is available. Every data transfer thus encompasses an integral number of memory blocks.

In MANUAL mode, only the ordered set of empty blocks within the set of selected blocks can be used to store data. In either AUTO or MANUAL mode, blocks that already contain valid data are skipped in the selection process. There is no restriction on the number of blocks that can be selected.

The WRITE sequence begins automatically whenever the "data input available" signal is presented - provided the "system busy" monitor is not asserted. In the latter case, if the system was in READ mode, the WRITE sequence is delayed until the READ operation is complete. Input data till that time will be lost. Once the "data input available" signal is interrupted, it should not be reasserted until the system busy signal is reset. Storage of each burst of input data begins in the first storage location of the next available memory block.

(3) During a data transfer, the CCD clocks to the accessed bank operate at $\frac{1}{4}$ the data rate. Retention of data recirculating in the dynamic CCD shift registers in the idle mode is performed by reducing the CCD clock rate to less than 20 KHz.

(4) Data is recovered from the memory by a READ operation, which can be performed destructively or non-destructively. Data in memory blocks that are read non-destructively (NDRO) is maintained and is available for further read-out. Memory blocks that are read destructively (DRO) have their block flags cleared so that access is permitted for a WRITE operation.

The READ sequence is initiated by selecting NDRO or DRO, selecting AUTO or MANUAL mode, selecting an ordered set of blocks to be read if in MANUAL mode, and then pressing the READ/WRITE pushbutton. The memory system reads-out in order all selected blocks whose flag have been set, thereby indicating that they contain data. If the READ mode is requested during a WRITE operation, the READ sequence automatically follows the end of the WRITE sequence. Data output is made available at the front panel BNC connector, is synchronized with the input clock, and is coincident with a LOW-true data output available signal. Data can be read at all specified clock frequencies, i.e., 150 KHz to 4.0 MHz.

All of the operating procedures are controlled manually on the feasibility model. The manual controls could be replaced by computer commands, and generally with considerable reduction in circuit complexity in the demonstration unit. A more detailed description of the system circuitry is presented in the following chapter.

III. DETAILED SYSTEM DESCRIPTION

3.0 Introduction

An evaluation of the feasibility of the memory system requires more detailed knowledge than simply that of the operating procedures and system specifications. A general description of the internal operation of the memory is given in this chapter along with an analysis of each block which comprises the system. Timing information is included wherever necessary for better understanding of system performance and operating limitations. A discussion of the logic device families that were used is related to theoretical and measured system power consumption.

3.1 System Description

In essence, the memory system takes a serial input data stream, routes the data to the first available memory block, and stores the data in successive memory locations. 32 blocks, each with a capacity of 4 K bits are available for data storage. Then upon command, the data in any memory block can be read on a first-in first-out basis and presented in serial fashion to the memory system data output terminal.

Complications to this basic design arise from the dynamic nature of the storage medium, recirculating CCD shift registers. An 8-bit counter, external to the CCD's, provides a virtual address (VA) for each storage location on the CCD shift registers, or tracks. The VA is incremented with each CCD transfer clock cycle, which is maintained at an idle rate for data refresh while the system is not being accessed. Data storage must always begin at the start address of any memory block. This start address is determined arbitrarily by the ZERO state of the virtual address counter, i.e., $VA = 0$. Since input data may arrive at any time, it is unlikely that the start of the incoming data stream will coincide with the memory block start address. The random start time of input data relative to $VA = 0$ necessitates the use of a pre-buffer that temporarily stores incoming data until it can be written into the CCD's after the memory block start address has been reached. The input pre-buffer is shown in relation to the other blocks in the system block diagram in Figure 3-1.

Further complications to the design of the pre-buffer and the CCD array are caused by the need to handle data rates in excess of the

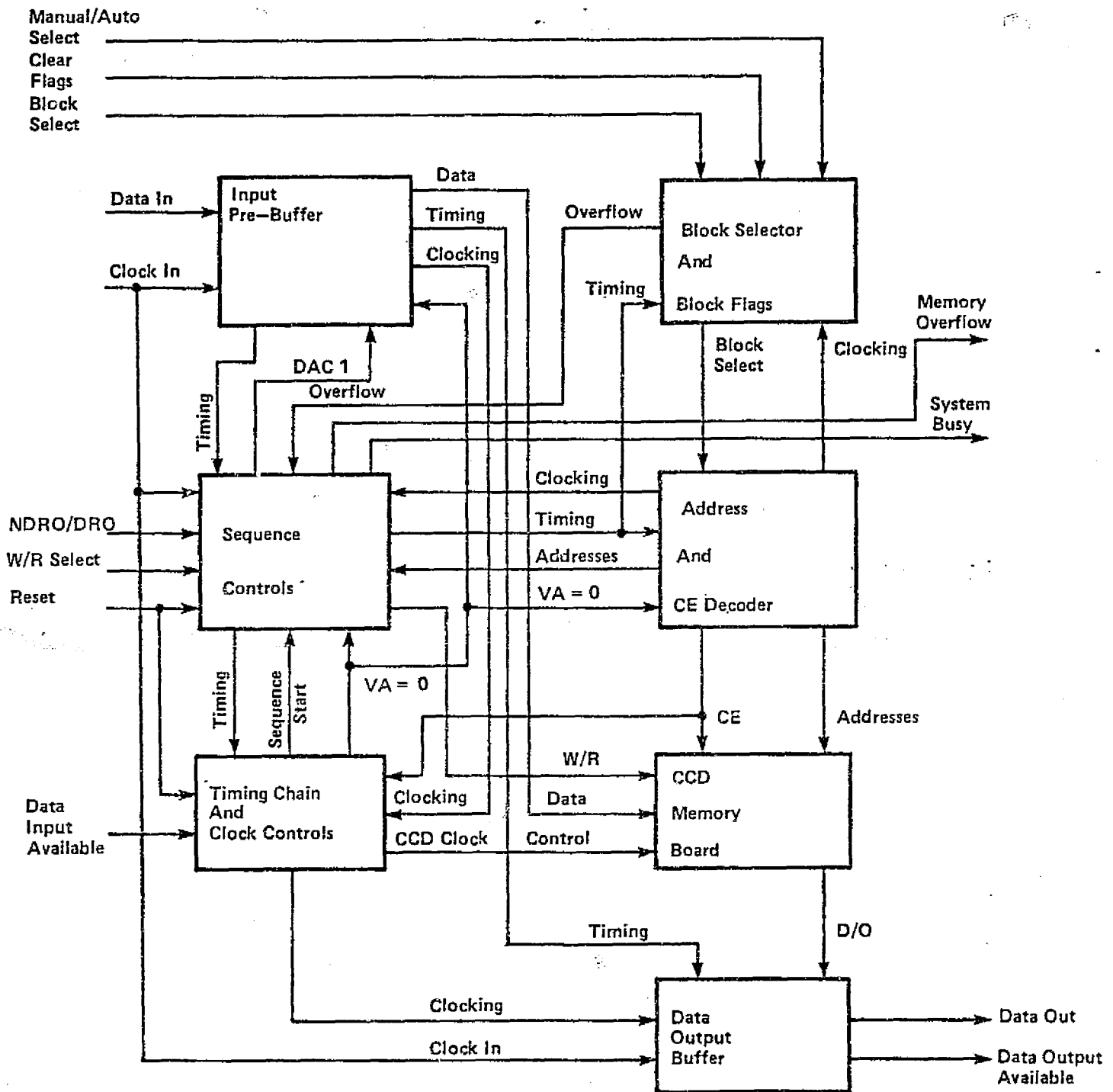


Figure 3 - 1 Block Diagram of Buffer Memory System

capability of individual CCD's. Since the 8K CCD is specified to operate at rates up to 1 MHz, 4-way data multiplexing was used to achieve data transfer rates up to 4 MHz. A serial-to-parallel data converter in the pre-buffer is used to route input data along 4 parallel paths to the CCD's. The CCD's are arranged in a 4 by 4 array to accommodate the parallel data inputs. Each bank of 4 memory devices is used to store 8 memory blocks. When the memory is being accessed, 4 bits of data - 1 for each device in a bank - are transferred simultaneously with every CCD clocking cycle.

The block selector logic plays a key role in the data routing process. In a WRITE operation, only empty blocks may be accessed; in a READ mode, only blocks containing data may be accessed. The selector examines the status of the block-in-use flags and the set of selected blocks to determine the first memory block that can be accessed. The signal representing the selected block is decoded as a 7-bit address which is latched into an address register at the beginning of a block transfer. While the transfer is taking place, the block selector searches for the next block to be accessed.

After a readout request has been made, the memory waits until the start address of the first memory block to be read is reached, and then it transfers 4 data bits at a time to a parallel-to-serial converter. In this way, the output is presented as a first-in first-out serial data stream.

Each of the portions of the memory system that have been mentioned and the blocks representing the sequence controls, timing chain, and CCD clock controls as shown in Figure 3-1 are described in greater detail in the following sections.

3.2 Input Pre-Buffer

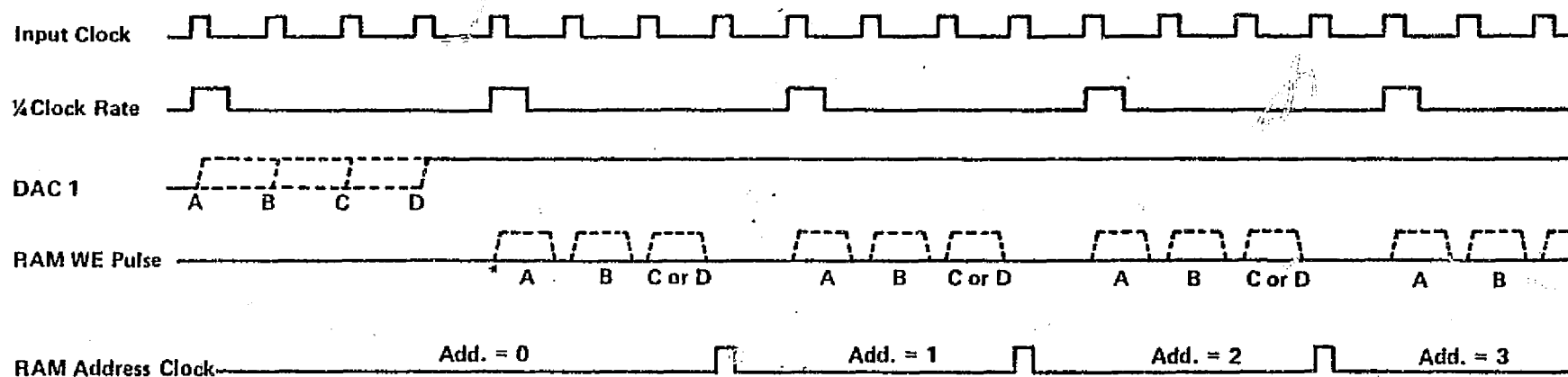
The input pre-buffer performs 2 basic functions. It performs a demultiplexing operation to convert the serial input data stream into 4 parallel paths. The pre-buffer also acts as an adaptable, variable-length shift register to synchronize the input data stream with the recirculating CCD memory storage locations. The schematic diagrams of the pre-buffer are shown on sheets 1 and 2 of Appendix C.

The input demultiplexing circuit consists simply of a serial-input, parallel-output shift register that is clocked by the input clock. A multiplexer is used to select either the 4 bits in the shift register or the direct input bit and the first 3 bits in the shift register. The selection of either of these sets of input data is governed by pre-buffer synchronization logic, to be discussed later. Each set of 4 input bits is stored in successive locations in 4 parallel RAM's, each with a capacity of 256 bits. The RAM's which were used were static, low-power, SOS CMOS RAM's from Inselek (INS 4200). Specifications for the INS 4200 RAM are given in Appendix D. RAM address and READ/WRITE controls comprise the remainder of the pre-buffer.

Since 4-way data multiplexing is used, a CCD timing clock is generated with every 4 input clock pulses. The start of an input data transfer initiates a data available control signal (DAC 1), which may be asserted at any input clock period within a CCD clocking interval ($\frac{1}{4}$ clock rate). These times are indicated at A, B, C, or D in the timing diagram of Figure 3-2. The system now waits until the first 4 data bits arrive before storing them into address 0 of the 4 parallel RAM's. The start point of DAC 1 fixes the position of the RAM data input strobe (RAM WE pulse) within a $\frac{1}{4}$ clock rate cycle so that successive 4-bit sets of data can be stored.

It may be noted in Figure 3-2 that the RAM WE pulse can occur in only 3 of the possible 4 timing intervals within a $\frac{1}{4}$ clock rate interval. The fourth position is reserved for a RAM read-out cycle immediately prior to the start of the next CCD clocking cycle (initiated by the $\frac{1}{4}$ clock rate pulse). Thus, when DAC 1 starts in positions A, B, or C, the data input strobe always begins 4 input clock cycles later. The last 4 bits in the demultiplexer shift register are stored in the RAM with each RAM WE pulse. If, however, the data input stream begins at position D, the input data is strobed into the RAM's during the same interval as if the data had begun arriving at position C. In this case, the 4-bit sets of data that are stored are taken from the input data directly and the first 3 bits in the data demultiplexer.

In the system idle state, the RAM address is held at 0. After the first set of 4 input bits are stored, the RAM address is incremented at the beginning



• Position of RAM WE Pulse Depends on Start Position of DAC 1

Figure 3 — 2 Pre-Buffer Start-of-Transfer Timing Waveforms

of the fourth input clock within a $\frac{1}{4}$ clock rate period, as shown by the timing diagram for the RAM address clock in Figure 3-2. Each set of 4 input bits is stored in successive RAM address locations until the start address ($VA = 0$) of a CCD memory block is reached. The first set of input bits is then read from the RAM at address 0 and presented to the CCD's for a storage (WRITE) operation. The next 4-bit set of input data overwrites the data previously held in RAM address 0. The RAM address increments and the READ/WRITE cycle repeats until the last RAM address that was reached before the CCD start address arrived. The RAM address goes back to 0 and the entire process repeats until a complete memory block or set of blocks has been transferred. In this way, the RAM pre-buffer acts as a multiplexed, variable-length shift register. An example of the pre-buffer WRITE/READ sequence, RAM address, and CCD virtual address is shown in Figure 3-3.

3.3 Timing Chain and Clock Controls

Figure 3-4 illustrates the clocking waveforms ϕ_1 , ϕ_2 , and ϕ_3 and the timing for other related waveforms used in the CCD operation. The waveforms illustrate a CCD READ followed by a WRITE operation.

The CCD timing chain trigger (T.C. Trigger) which initiates the transfer clocking cycle is generated from the $\frac{1}{4}$ clock rate signal. Each cycle begins by resetting the ϕ_3 clock and latching new values of chip enable (CE) and track address. Timing specifications for the T.C. trigger - which determines the ϕ_2 set-up time - and the ϕ_1 , ϕ_2 , and ϕ_3 clocks are given in Appendix A. The CCD virtual address of the next clocking cycle is changed at the beginning of the ϕ_3 clock. The virtual address is out of step with the track address since it has no direct control of the CCD's and it is used in some of the control logic which must be set up before the end of the ϕ_3 clock.

In a READ cycle, the data output becomes valid shortly after the rise of ϕ_3 and is normally held until the start of the next ϕ_3 . If data is to be stored in the CCD, the CE and track address are asserted during the first CCD clocking cycle and the WRITE and data input are presented to the CCD's at the beginning of the next cycle (as shown in Figure 3-4). This feature of the CCD write

RAM Address	0	1	1	2	2	3	3	4	4	0	0	1	1	2	2	3	3	4	4	0	0	1
RAM W/R Operations	W	—	W	—	W	—	W	—	W	R	W	R	W	R	W	R	W	R	W	R	W	R
CCD Address	252		253		254		255		0		1		2		3		4		5		6	
CCD Operation*	—		—		—		—		—		W		W		W		W		W		W	

* Write Data Into Previous CCD Address

Figure 3 — 3 Example of RAM Address, RAM and CCD W/R Operations, and CCD Virtual Address Sequences

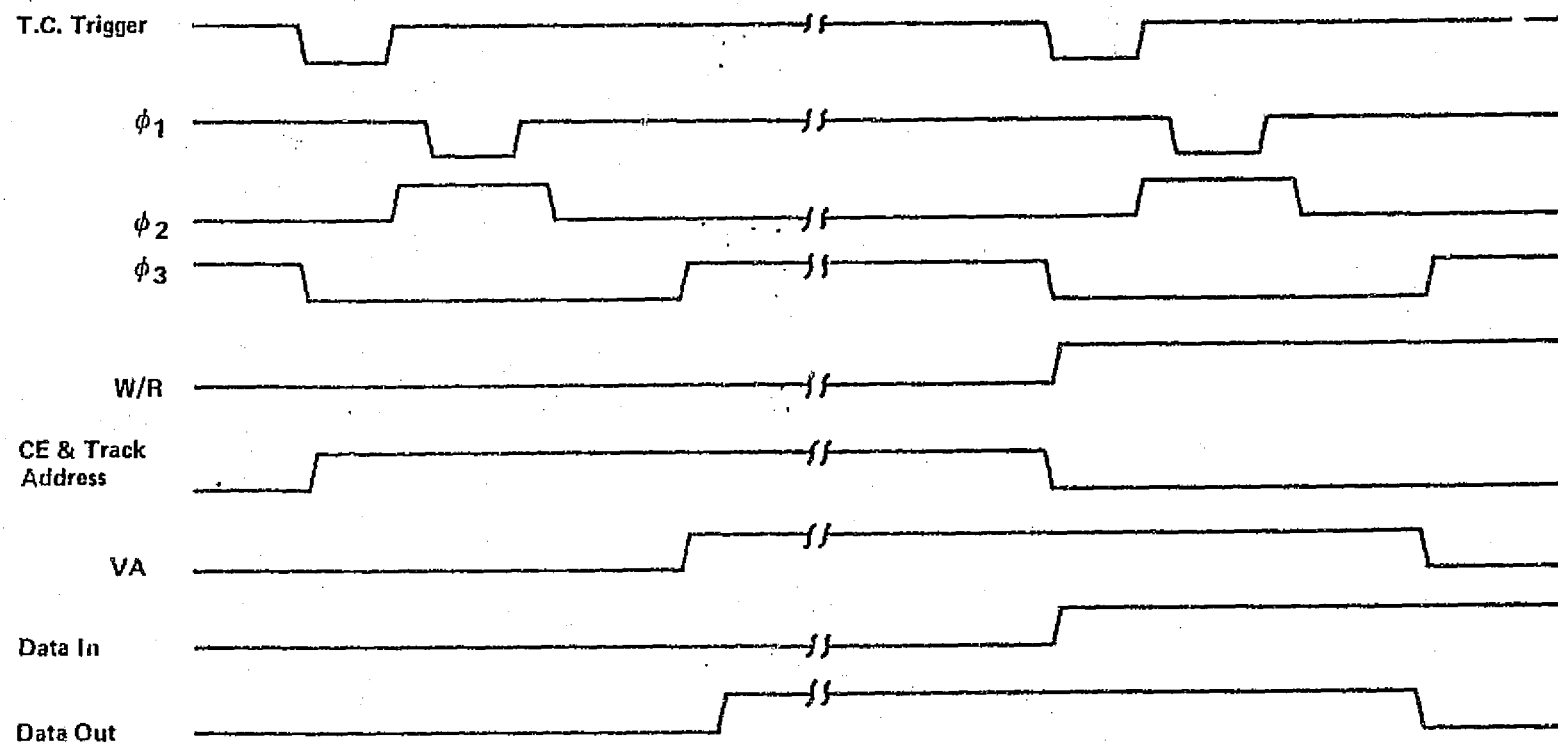


Figure 3 — 4 CCD Timing Signals

operation allows time for the RAM pre-buffer to detect the start address ($VA = 0$) of a CCD memory block, READ the first set of 4 bits from the RAM's, present the data to the CCD's, and then store the data into the 0 address. Thereafter, each set of data will be stored in the proper, successive CCD storage locations.

Controls are designed for the CCD clocking to operate in 3 modes; idle, transfer set-up, and data transfer mode. When the system is in the idle state, that is not undergoing a data transfer, the CCD's should be clocked at rates between 10 KHz and 20 KHz to keep data refreshed and to minimize power consumption. Clock pulses from the $\frac{1}{4}$ clock rate signal are gated by an idle rate control oscillator to form CCD T.C. trigger pulses at an average rate of less than 20 KHz. Figure 3-5 illustrates the timing involved in generating the idle rate trigger. The duration between T.C. trigger pulses could be either t_1 or t_2 (see Figure 3-5), depending on the phase relationship between the idle control oscillator and the $\frac{1}{4}$ clock rate. The idle control has been adjusted so that $t_1 \approx 56 \mu\text{sec.}$ and $t_2 \approx 83 \mu\text{sec.}$ when the input clock rate is 150 KHz. These times correspond to maximum and minimum idle rates of 18 KHz and 12 KHz, respectively. As the input clock increases to 4 MHz the difference between t_1 and t_2 becomes negligible. The idle rate then becomes approximately 15 KHz.

When a request for data transfer is initiated, the idle mode control of the $\frac{1}{4}$ clock rate is immediately overridden. All $\frac{1}{4}$ clock rate pulses pass through the idle control gating to form T.C. trigger pulses. Since input clock rates may vary from 150 KHz to 4.0 MHz, the CCD clocking rates may range from 37.5 KHz to 1.0 MHz, respectively. In order to reduce system power during a transfer operation, only the accessed memory bank operates at the above transfer rates. All memory banks are clocked at the same rate during the idle mode and after a request for data transfer has been made, until the start address for a transfer has been reached (transfer set-up mode). Then the clocking rate of all non-accessed banks is reduced to a quarter of the clocking rate of the accessed banks. Thus, non-accessed memory banks operate at 9.375 KHz to 250 KHz rates during a data transfer. The CCD clocking rates and the address sequences for all modes of operation are illustrated in Fig. 3-6.

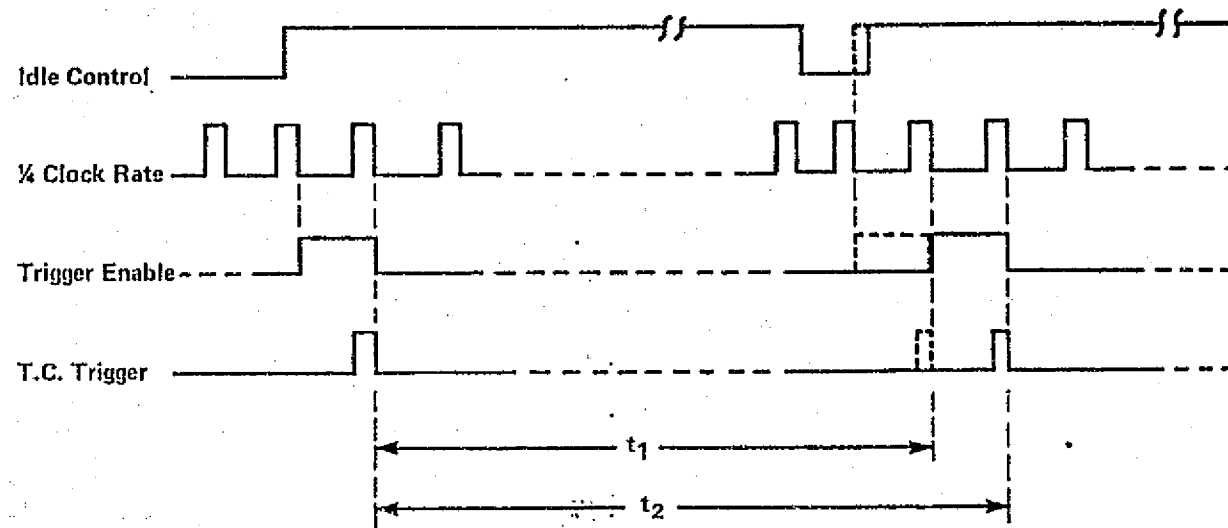


Figure 3 — 5 T.C. Trigger Idle Rate Timing

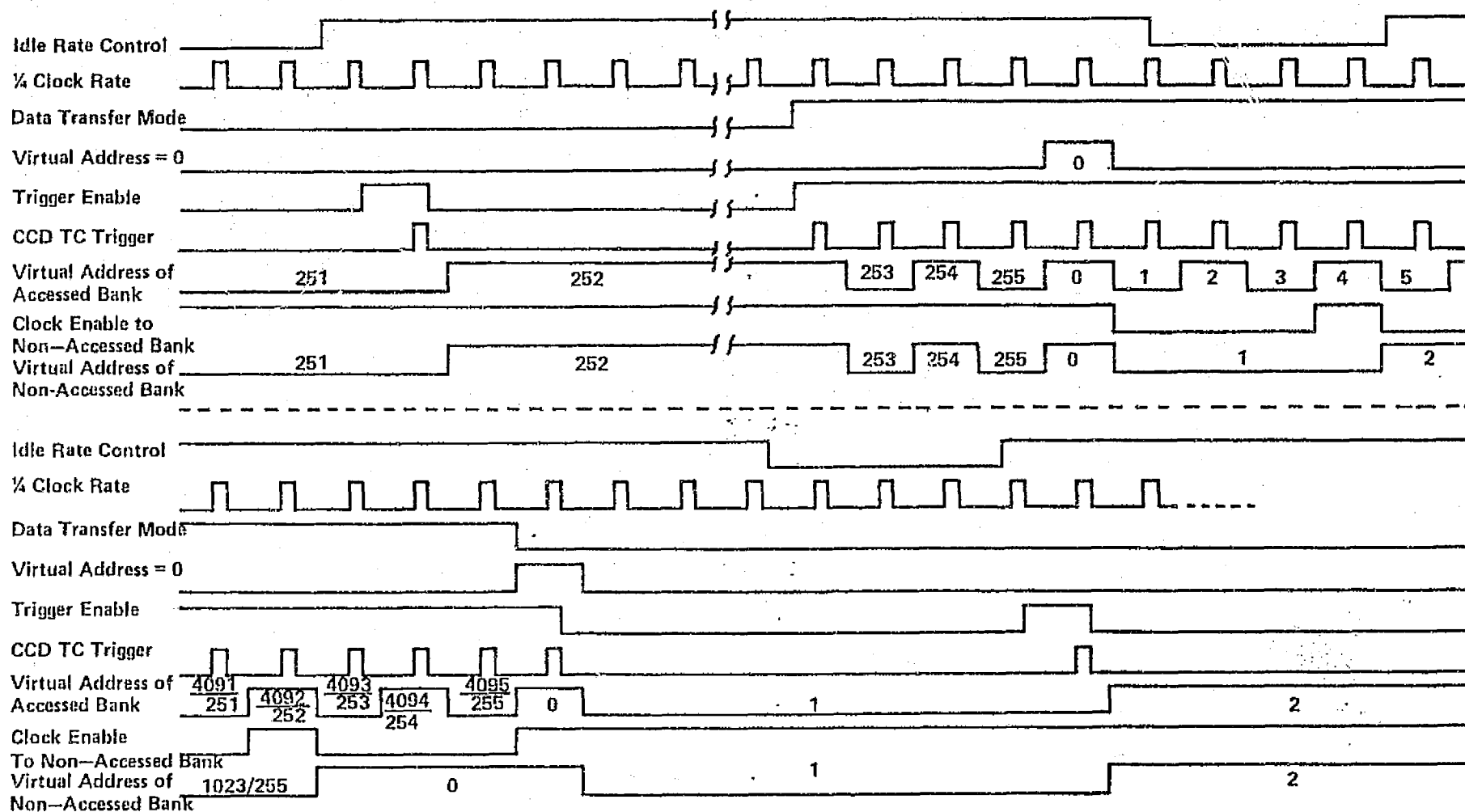


Figure 3 — 6 CCD Clock Trigger and Address Sequences

The length of a memory block is 4096 bits, whereas a CCD track contains 256 bits. Therefore, by clocking a non-accessed memory bank at $\frac{1}{4}$ the access rate, non-accessed tracks recirculate 4 times during a memory block transfer. The virtual address of tracks in both accessed and non-accessed memory blocks are again synchronized at the end of a data transfer. This is illustrated in Fig. 3-6. The dual address labelling (eg. 4094/254) towards the end of the transfer denotes the number of CCD transfers and the virtual address of a CCD track.

3.4 CCD Memory Board

All of the CCD storage devices are located on one board, together with all clock, address, chip enable, and R/W drivers. The schematic for the 4 by 4 array of 8K CCD's is shown on sheet 4 of Appendix C. A photograph of the CCD memory board is shown in Fig. 3-7. The board has 4 parallel data inputs, with corresponding data outputs. Data outputs, which are TTL compatible, are complementary outputs.

Since the clock lines to the CCD's represent high capacitive loads, high power TTL-to-MOS drivers (MH0026) are used to drive the ϕ_1 , ϕ_2 , and ϕ_3 clock inputs. Each of the ϕ_1 and ϕ_2 drivers operate 2 CCD's. The ϕ_3 driver operates 4 devices. Rise and fall time degradations limit the system performance if the drivers are loaded with more devices. Specifications for the MH0026 drivers are provided in Appendix E.

3.5 Block Selector and Flags

Versatility of memory block access is provided by an iterative array of block selector cells and block flags. Schematic diagrams for this portion of the system are given on sheets 7 to 14 of Appendix C.

A block flag is set whenever the memory block associated with it contains valid data. It can be reset by a manual command or by a destructive readout operation.

Each cell of the block selector logic examines signals that indicate if a memory block has been selected for a possible transfer operation, the current status of its associated block flag, and whether or not all lower order memory blocks are available for data transfer. During a WRITE operation, if the block has been selected for a transfer, if the block flag is not set, and if no lower order blocks are available, then the

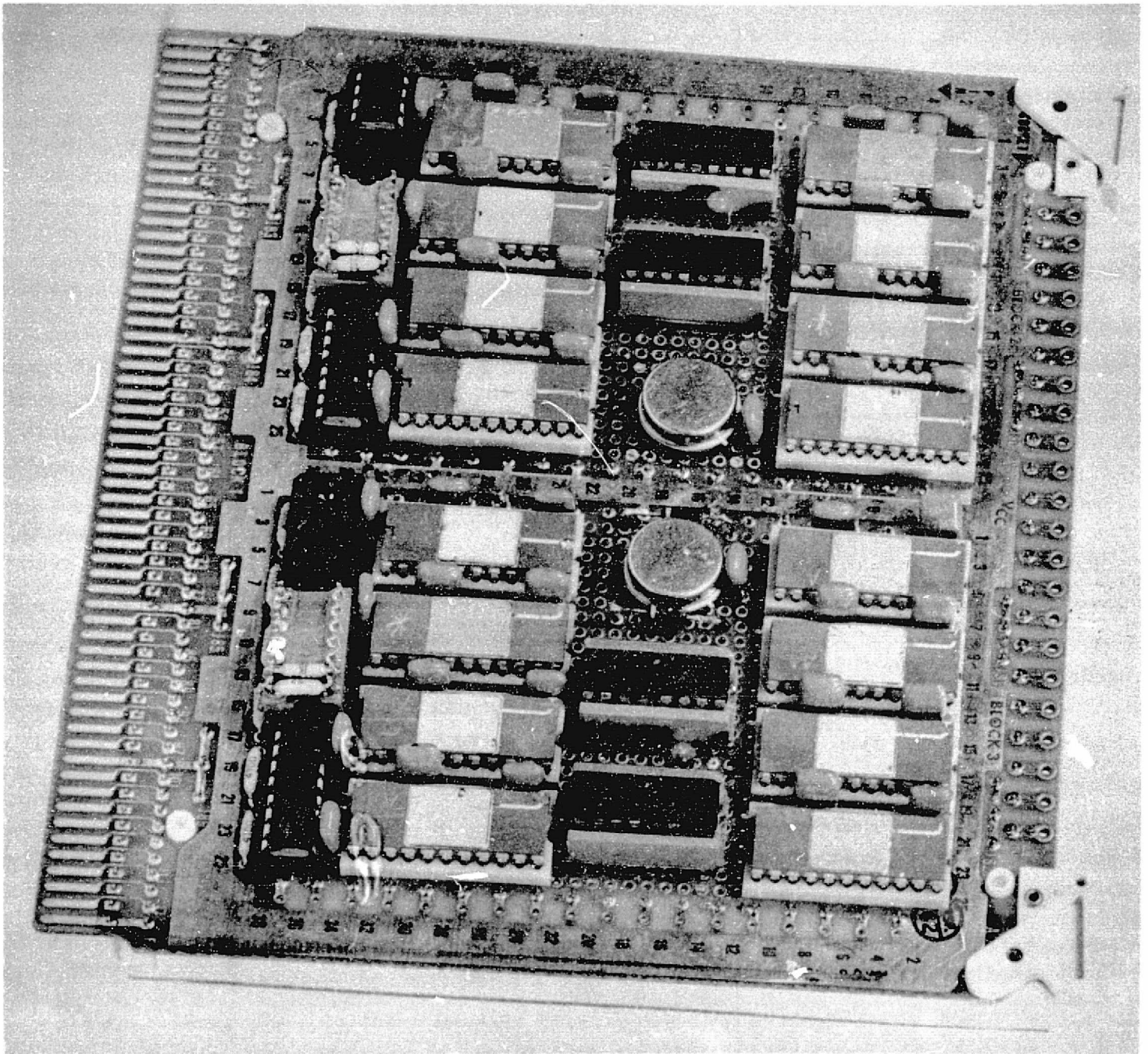


Figure 3-7: 128 K-Bit CCD Memory Board

block selector cell asserts its "block selected" signal. Only 1 out of the 32 selector signals can be asserted at any time. When the data transfer to the selected block begins, the block flag is set. This action inhibits the block selector signal and sets up an enable signal to the next, higher order block selector cell.

During a destructive readout operation, the complement of the block flag is sent to the block selector circuitry so that only memory blocks that contain valid data can be read. As each block is selected for a READ operation, the block flag is reset.

Since the flag must not be reset during a non-destructive READ operation, an auxiliary flag is used for the block selector control. The auxiliary flag is set at the beginning of the block transfer and is used to indicate to the block selector that the block has been read. If the auxiliary flag were not used, there would be no change in the block flag or block selector signals so that the system would repeatedly read the same block. All auxiliary block flags are reset at the end of a system READ operation.

At the end of a READ operation, when all flagged blocks from a selected set of blocks have been read, a selector overflow signal is asserted to indicate the end of the READ cycle. The overflow signal is asserted during a WRITE operation only when no blocks are available to store more input data.

3.6 Address and Chip Enable Decoder

The block selector prepares for a data transfer by selecting the next block to be accessed. It asserts 1 out of 32 block select lines. The address and chip enable decoder, shown on sheet 6 of Appendix C, decodes the block select lines to form a 3-bit CCD address and a 4-bit chip enable coder. The chip enable code selects 1 out of 4 CCD banks for access. The 3-bit CCD address is a binary code which determines the memory block within a CCD bank that is to be accessed. This 3-bit code addresses the most significant bits of the 5-bit CCD track address. The decoded block select addresses are latched into a register and presented to the CCD memory board only at the beginning of each memory block transfer.

The remaining 2 bits of the CCD track address are used to sequence through the 4 tracks on each CCD which comprise a single memory block. The 2 bits, A_0 and A_1 , are determined by the output of a Gray code counter which is indexed each time the $VA = 0$ signal is asserted after the beginning of a block transfer. Since the A_0 and A_1 signals are also used for sequence controls, a Gray code count is used to avoid hazard conditions.

3.7 Data Output Buffer

The data output buffer, shown at the bottom of sheet 5 in Appendix C, is used to convert the 4-bit parallel CCD output into a serial data output stream. Approximately 150 nsec. after the rise of a ϕ_3 signal, the CCD data outputs are latched into a 4-bit buffer. The output of this buffer is transferred to another 4-bit register at the beginning of the next CCD transfer cycle. Timing diagrams related to the output buffer circuit are shown in Fig. 3-8. After the 4 parallel bits have been latched into the second buffer, each of the data bits in this register is selected in turn by a multiplexer (MUX) whose output is sent to a single bit register. The output of the single bit register, which is clocked by the input clock, provides the first-in, first-out, serial data output stream. For the duration of a valid data output, a LOW-true data output available signal is asserted.

3.8 Sequence Controls

A number of signals are generated to control the sequence of operations within the system. The principle control signals are the READ/WRITE, the data available controls (DAC), transfer request, system busy, and memory overflow. The circuits to generate these signals are shown on sheet 5 of Appendix C.

The system is normally prepared for a WRITE operation; that is, in the idle state, the WRITE signal is asserted. However, no CCD operation takes place since the chip enable lines are inhibited. If a READ operation is requested, the READ request is latched and held until all available memory blocks that have been selected are read once. If a READ request is made during a WRITE operation, the system waits until the end of the data input transfer before it proceeds with a data output transfer. Similarly, a WRITE request is blocked until the end of a READ operation.

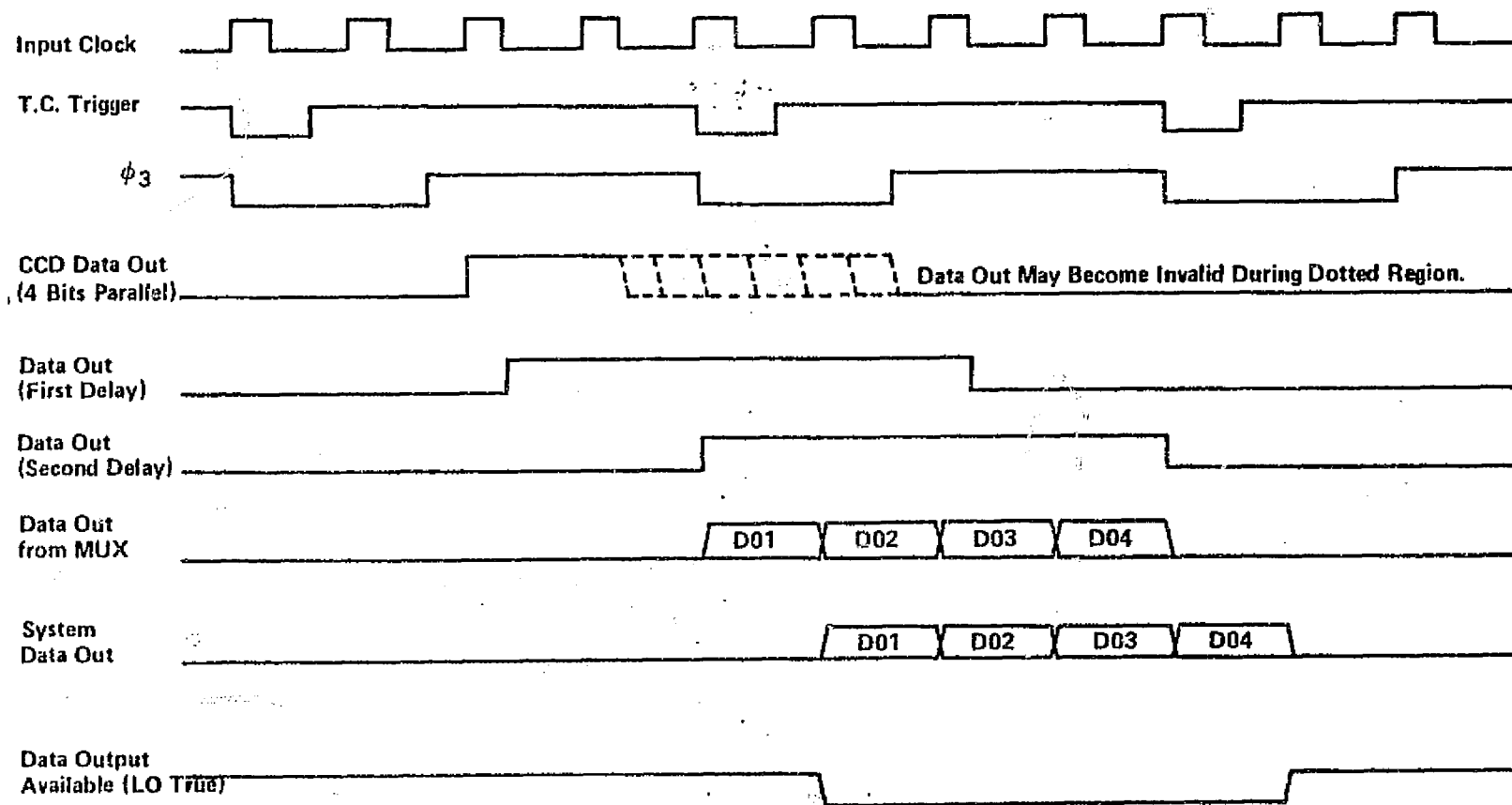


Figure 3 – 8 Data Output Timing

Since a data input burst length may not coincide with a CCD memory block length, DAC (data available control) signals are set up to ensure that the system operation continues until the end of a CCD memory block is reached. Whereas the DAC signal is asserted from the beginning of a request till the end of a data transfer, the transfer request signal is used to control a number of system operations that take place only during the actual data transfer. The system busy signal is used both as a monitor and to block a READ request during a WRITE operation or to block a WRITE request during a READ operation. The memory overflow signal is also used as a system monitor, and as a control to signal the end of a READ operation or the lack of available memory blocks during a WRITE operation.

3.9 Power Consumption

Several device families are used in the system implementation; TTL, low-power Schottky TTL, CMOS, CCD's, and TTL-to-MOS drivers. Since CMOS logic and MOS drivers with a high capacitive load are used in the system, the power dissipation varies with input clock frequency. System idle power is approximately 5.4 W, whereas peak operating power is approximately 7 W. These values result in a power consumption/bit of 41 μ W and 53 μ W during idle and maximum rate transfer operations, respectively. Estimated power consumptions for each device family are listed in Table 3-1. Measured power dissipation curves for a number operating modes and over the operating range of frequencies are shown in Fig. 3-9.

Device Family	Power Estimate During Idle (W)	Power Estimate During 4MHz Data Transfer (W)
TTL	1.01	1.01
LS TTL	1.73	1.73
CMOS	negligible	.14
8K CCD's	.39	.39
MOS Drivers	<u>1.94</u>	<u>3.79</u>
Total Estimated Power	5.07 W	7.06 W
Total Measured Power	5.39 W	6.95 W
Actual system power/bit	41 μ W	53 μ W

Table 3-1 System Power Dissipation

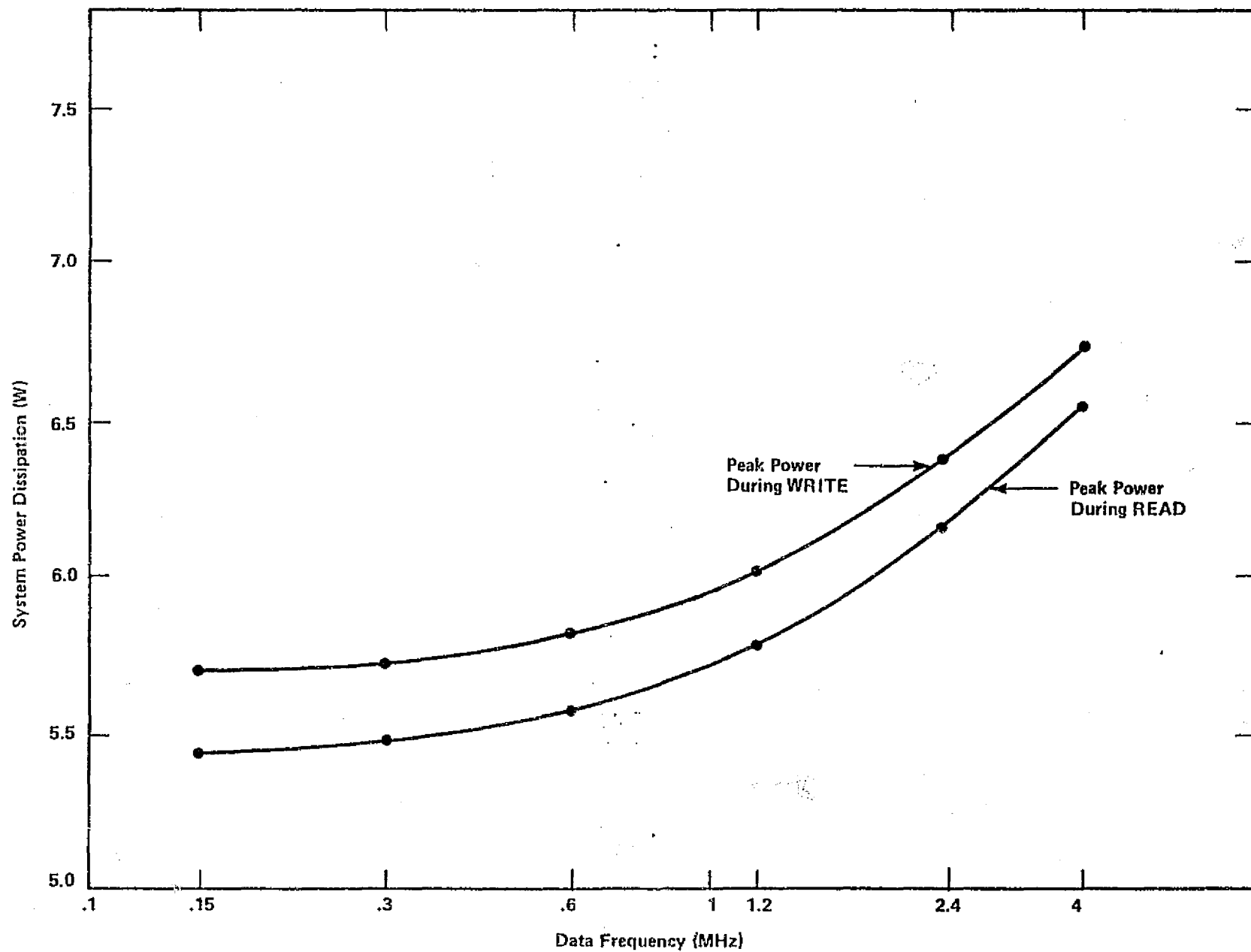


Figure 3 — 9 Total Power Dissipation in READ and WRITE Modes vs. Data Rate

The system power dissipation has not yet been optimized. Some of the logic that is presently implemented with TTL logic could be replaced with CMOS logic. Additional control of the CCD clock drivers could be introduced to reduce DC power consumption of the drivers during the idle mode. It is expected that the system idle power could be reduced to less than 4 watts with a corresponding decrease in the operating power. If the system were redesigned to operate under computer control, the idle power dissipation should fall to less than 2 watts. Any stand-alone system configured as described would lend itself to the extensive use of custom LSI CMOS which would permit significant reduction in power and space. The repetitious nature of many of the modules particularly suggests such an approach.

IV. MEMORY SYSTEM EXERCISER

4.0 Introduction

Due to the complexity and versatility of the memory system it was necessary to design and construct a custom exerciser to adequately test the system. The exerciser would have to perform pattern sensitivity and memory integrity tests as well as standard operational and margin tests. Consequently the tester has been designed to generate and write a number of data patterns into the memory under test (MUT), varying from a simple repeating pattern to a complex pseudo-random data pattern. Provision has also been made to replace 7 bits of any data pattern at specified intervals with an address code to test for memory integrity. In WRITE mode the exerciser can be set up to wait for specific states within the MUT prior to writing data. This ensures testing for correct operation of the memory in a variety of start-up conditions. In READ mode the exerciser operates slaved to the MUT to analyze the serial data output stream of the memory. Errors in the data stream are detected, counted, and the total is displayed on the front panel. The exerciser performs a test of a specific length once for every request.

Limits of the MUT can be tested by varying the operating frequency of the exerciser, thereby varying the tester data rate. To increase flexibility of the test, not only the data pattern but the length of that pattern is variable. This allows sections of the memory to be tested individually, as well as allowing for various size memory systems.

To ensure that testing is reliable and repeatable the specifications of the exerciser must exceed those of the memory to be tested. The primary tester limitation, speed, is at least double that required for the CCD memory system under consideration here.

In this chapter the specifications of the tester will be put forth and the operating procedure will be explained.

4.1 System Specifications

a) Clock Output:

Repetition rate: 9.6 MHz max.

Pulse width: 35 nsec. min.

Level: $2.0 \leq \text{high} \leq 4.7$ V; $\text{low} \leq 0.4$ V

Drive capability: ≤ 20 mA @ 4.7 V

Source: Internal - Crystal-controlled

- rate divisible in binary steps

External - Continuously variable

b) Data Output:

Data type: Non-return-to-zero (NRZ)
 Level: $2.0\text{ V} \leq \text{high} \leq 4.7\text{ V}$; $\text{low} \leq 0.4\text{ V}$
 Drive Capability: $\leq 20\text{mA}$ @ 4.7 V
 Pattern length: 2^{21} bits max.
 2^3 bits min.

c) Data Input:

Threshold: TTL compatible
 Valid: Rising edge of clock out
 Loading: One TTL load

d) External Clock Input:

Repetition Rate: 9.6 MHz max.
 Pulse width: 35 nsec. min.
 Threshold: TTL compatible
 Loading: One TTL load

e) External Data Source:

Threshold: TTL compatible
 Valid: Rising edge of clock out
 Loading: One TTL load

f) Data Output Available:

Type of signal: Low true
 Drive capability: TTL compatible

g) Data Input Available:

Type of signal: Low true
 Loading: Five TTL loads

h) General:

Power: $+5\text{ VDC} \pm 5\%$ @ 3 Amps
 Operating environment: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$

4.2 Front Panel Controls and Functions

This section will list controls on the front panel and outline their functions. Refer to the photograph in Figure 4.1 and page 5 of Appendix F for the wiring diagram of the front panel.

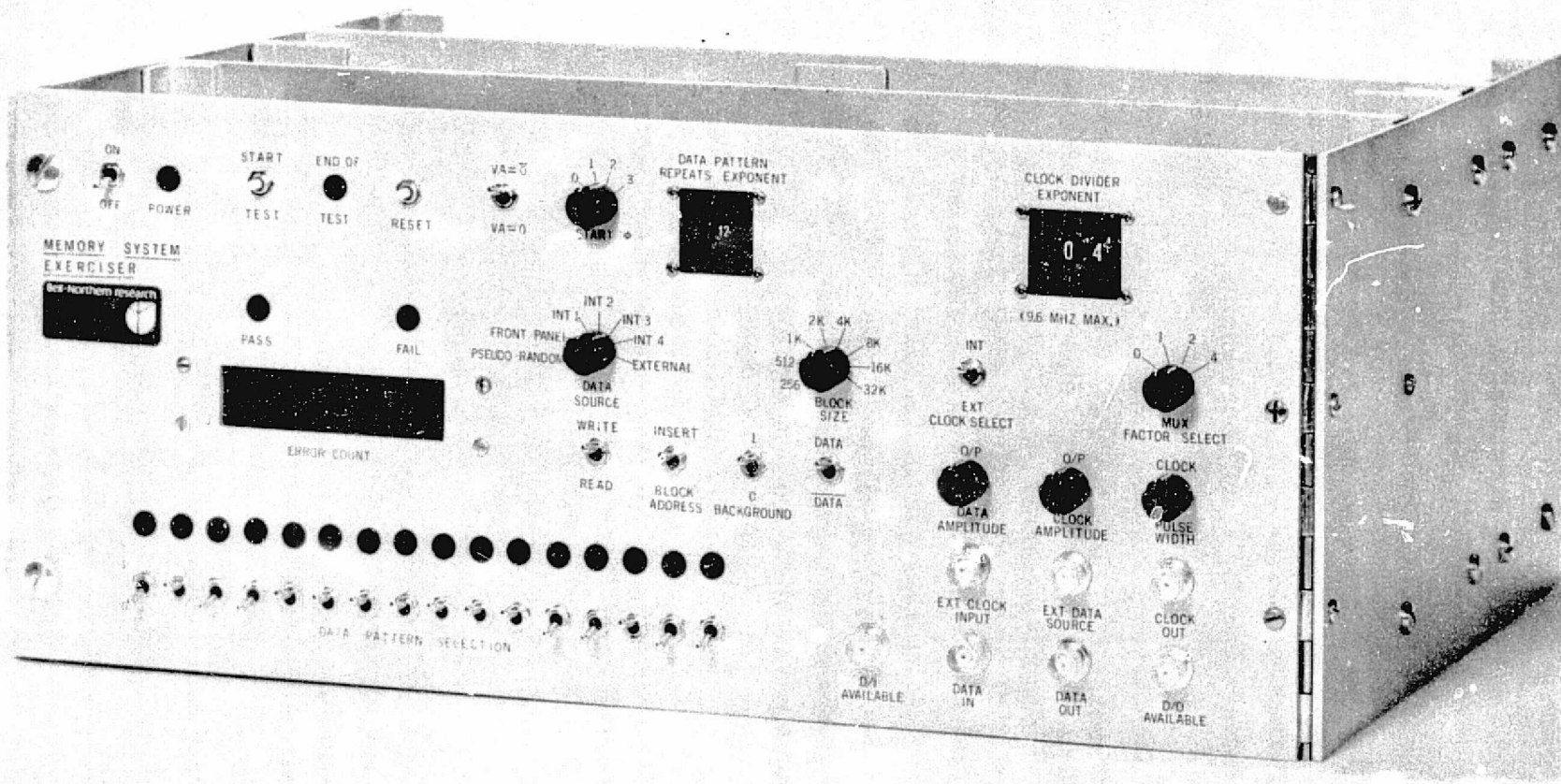


Fig. 4-1 Memory System Exerciser Front Panel

a) Switches:

1. Power (SPDT toggle switch)
 - Switches V_{CC} to the circuit boards and front panel.
2. Reset (momentary-contact pushbutton)
 - Initializes the test system prior to any test. The tester is held in its quiescent state until the Start Test button is depressed.
3. Start Test (momentary-contact pushbutton)
 - In WRITE mode the activation of this button signals the exerciser to begin sending data to the MUT. In READ mode it primes the exerciser to receive data from the MUT.
4. WRITE/READ (SPST toggle switch)
 - Determines the mode of operation of the tester. In WRITE mode the Data Output Available signal is asserted signifying that valid data is being presented to the memory. In READ mode when the Data Input Available signal is asserted, data presented to the tester is analyzed and the errors counted.
5. $VA = 0 / VA = \overline{0}$ (SPDT toggle switch)
 - Engaged in WRITE mode only, it determines where data output starts. In $VA = 0$ mode data output consistently starts in the same place relative to the memory system virtual zero address whereas in $VA = \overline{0}$ mode the start is random, related only to when the Start Test button is pushed.
6. Start Phase (4 position 2 pole rotary switch)
 - Used in WRITE mode only, it designates in which phase the data output pattern of the exerciser starts. It can be used in conjunction with the $VA = 0$ circuit for precise data start location.
7. Clock Divider Exponent (dual BCD thumbwheel switch)
 - Determines the frequency of operation of the exerciser in internal mode and the Clock Out to the MUT using the formula $\left(\frac{9.60 \times 10^6}{2^n} \right)$ Hz, where $0 \leq n \leq 17$. (Caution: the Clock Output maybe interrupted during switching).

8. Clock Select (SPDT toggle switch)
 - Determines which clock is chosen, the internally generated, crystal-controlled, logically-divided clock or an external clock which is brought in from a front panel connector.
9. Data Source (7-position, 2-pole rotary switch)
 - Selects which of 7 sources of data will be used to supply data to the MUT. These sources include a pseudo-random generator, a bank of 16 switches on the front panel, 4 banks of 16 switches (labelled INT 1, INT 2, INT 3, INT 4) internal to the memory exerciser, and an external data source supplied from a connector on the front panel.
10. Data Pattern Selection (16 SPDT toggle switches)
 - These switches determine the pattern of a 16-bit test word. This pattern can be repeated to form the data output of the exerciser.
11. MUX Factor Select (4-position, 2-pole rotary switch)
 - Each data bit can be held for 1, 2, or 4 clock periods as determined by this switch. In this way the parallel paths in a multiplexed memory system can be tested with the same data pattern simultaneously.
12. Data Patterns Repeats Exponent (16-position binary-coded thumb-wheel switch)
 - This switch is a prime factor in determining the length of the data pattern. The length of the data pattern is determined using the formula $(2^n \times \text{MUX Select} \times 16)$ bits where data pattern repeats exponent is n and $0 \leq n \leq 15$ for all data patterns except pseudo-random. Because of the structure of the pseudo-random generator the data pattern length is determined by halving the above formula. The pseudo-random pattern depends on the length selected.
13. Insert Block Address (SPDT toggle switch)
 - Allows for the replacement of data with a unique 7-bit code at the beginning of every memory block. For this CCD memory system the code consists of 4 bits to indicate the accessed CCD bank and a 3-bit binary code to represent which of the 8 blocks in that bank is selected.

14. Block Size (8-position, 2-pole rotary switch)

- This switch is set to the number of storage locations in each memory block, from 256 to 32 K. This determines the number of clock intervals between block address code insertions into the data stream.

15. Data/ $\overline{\text{Data}}$ (SPST toggle switch)

- Permits the exerciser data output to be complemented.

16. Background (SPST toggle switch)

- Determines the output data logic level which follows the completion of the data pattern.

b) Potentiometers:

1. Clock Pulse Width (50 K Ω)

- Is used in conjunction with a monostable multivibrator for control of variable pulse width of clock out (35 ns to 400 ns).

2. Output Clock Amplitude (10 K Ω)

- Used as part of a diode clamp circuit, it allows a variable high level of the Clock Out from 2 volts to 4.7 volts.

3. Output Data Amplitude (10 K Ω)

- Similar to the output clock amplitude, a diode clamp network allows a variable high level from 2 volts to 4.7 volts.

c) Lamps:

1. Power (LED)

- Indicates, when ON, that power is being delivered to the circuit boards and front panel.

2. End of Test (LED)

- When ON, indicates that a test sequence, either READ or WRITE, has been completed and the exerciser is in its quiescent state.

3. Pass (LED)

- In WRITE mode this light should come on with the End of Test light. In READ mode it indicates that the MUT has successfully stored and reproduced the data originally written into it.

4. Fail (LED)

- In WRITE mode this lamp should not light; if it does there is a fault in the memory exerciser. In READ mode, when lit, it indicates that the MUT contains one or more bits in error.

5. Error Count (DL-707 Seven Segment LEDs)

- In WRITE mode it should always contain a single zero; any other condition indicates a fault in the exerciser. In READ mode it indicates the number of bits read from the memory

system which differ from the data originally written. Although the display employs reverse ripple blanking, at least one digit, the least significant, should be visible at all times.

6. Data Pattern Selection (16 LEDS)

- Displays the 16-bit pattern selected on any one of the switch registers, internal or front panel, ON indicating a high. In external or pseudo-random data source modes the display should not be lit.

d) Connectors:

1. External Clock Input

- This connector allows an external clock generator to operate the exerciser and memory system. This permits the variation of clock frequency and pulse width in a continuous scale.

2. External Data Source

- It permits the usage of data from a source other than the exerciser.

3. Clock Output

- The clock in the memory exerciser is provided for use as the input clock of the memory system under test.

4. Data Input Available -

- Is used to signal the exerciser that the memory system is sending valid data on the data input line. In READ mode this starts the generation of data for a comparison with that data being received. In WRITE mode this signal line is ignored.

5. Data In

- Data sent by the MUT is received at this connector.

6. Data Out

- The exerciser uses this connector to send data to the MUT.

7. Data Output Available

- This signal when low informs the MUT that the data at the Data Out connector is valid.

4.3 Back Panel Controls and Functions

a) Power

- Banana connectors labelled +5 and GND designate and V_{CC} input to the memory exerciser.

b) Block Address

- This connector accepts information which is inserted into the data pattern to enable memory integrity tests to be performed. The information required for this operation is 7 signals representing a memory address code. The address codes for both the present block which is accessed and the next block to be accessed are required.

c) Virtual Address

- This connector accepts information to determine the start of the data stream relative to the zero address of the memory device. The signals required for this function are one defining the position of the zero address of the memory ($VA = 0$), two to determine the position (phase) in the 4-bit multiplexed data stream (GRO and GRI), and one to define the start of the multiplexed memory clocking cycle (Timing Chain Trigger).

Although the data starts at virtual address zero when the switch is in the $VA = 0$ position the start position can be moved to any address. This is accomplished through manipulation of an 8-switch SPST DIP package on the VA Board, which controls the load terminals of a counter. A binary count is set on this switch with the LSB on switch number 8. A binary ONE is set with the switch in the ON position. The present setting with a count of 15 corresponds to a start at memory virtual address 0. If X is the binary switch setting, then the corresponding virtual address at the data start will be $(241 + X) \bmod 256$.

When memory systems other than the CCD memory buffer are to be tested, or when it is desired to disengage the $VA = 0$ and Start Phase circuitry, a program socket must be changed. This socket, Clock Board device A1, should be inserted with its pin 1 mated with pin 1 of the circuit board socket to disengage the start address and phase logic. The data output will then start at a random address and phase. The program socket is reversed to engage the address and phase logic.

4.4 Exerciser Operating Procedures

References to the basic block diagram, Figure 4.2 will be made in explaining the exerciser operating procedures, detailed schematics of the

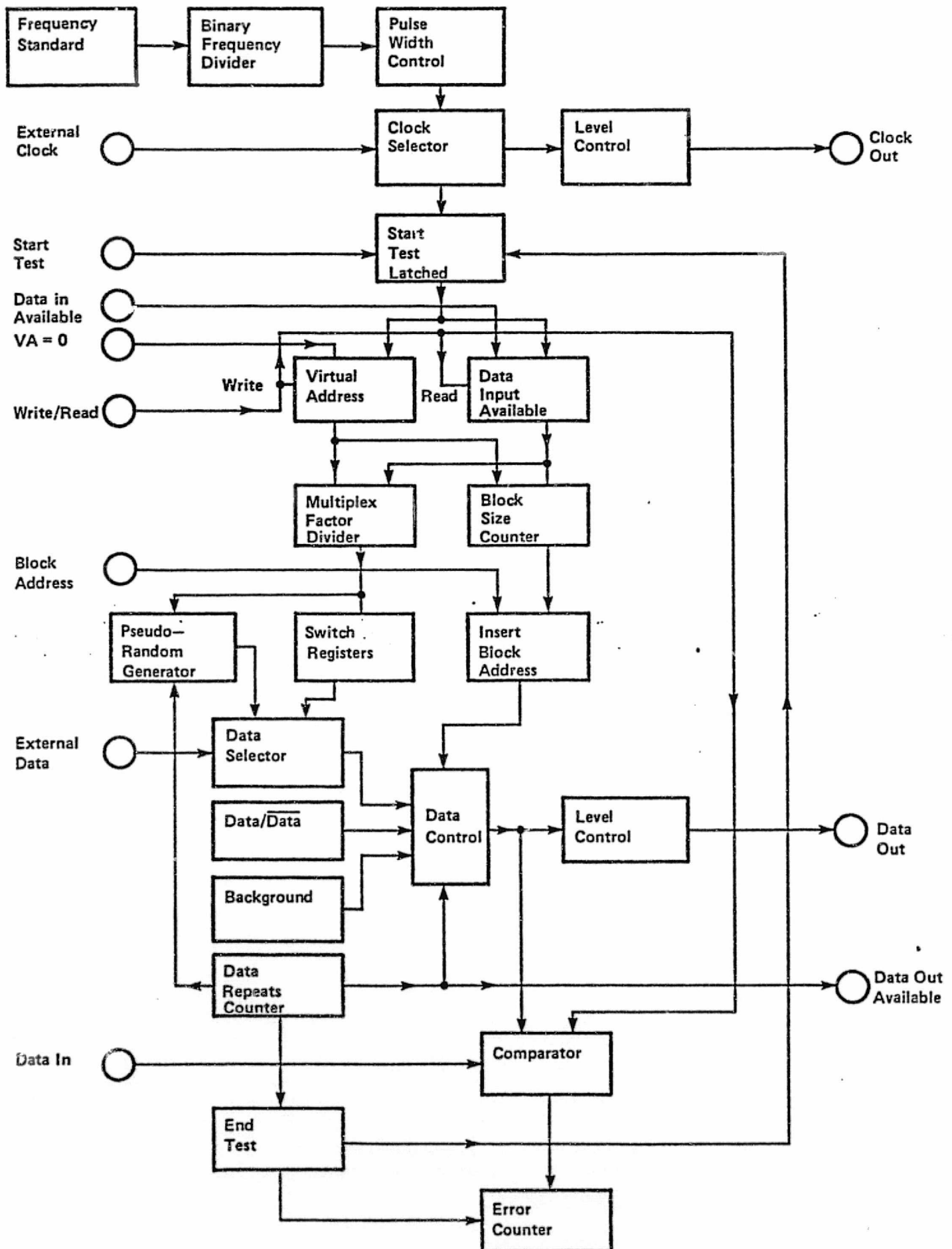


Figure 4 – 2 Block Diagram of Memory System Exerciser

system are provided in Appendix F. This section will cover the procedures for both WRITE and READ modes of the exerciser.

4.4.1 Start-up Procedures

These procedures are standard and must be followed prior to testing any memory system. Power must be applied to the V_{CC} connector on the back panel. Interconnections between the memory exerciser and the memory system should be made via the BNC connectors on the front panel and the amphenol connectors on the back panel. If an external clock or data source is to be used they should be connected to the front panel BNC connectors. At this point the power switch can be turned on and the frequency and pulse width of the clock should be adjusted. The frequency of the internal clock can be selected in binary submultiples of the 9.60 MHz frequency standard by using the Clock Divider Exponent switch. The clock pulse width can be adjusted using the potentiometer on the front panel. If an external clock is selected the frequency and pulse width of the Clock Out are those of the external pulse generator. Regardless of which clock source is selected the amplitude is controlled by a potentiometer on the front panel. The WRITE/READ switch should be placed in the WRITE position in preparation for a WRITE operation.

4.4.2 WRITE Mode Procedures

Prior to a WRITE operation all variables must be assigned values. Following the block diagram the first variable encountered is the virtual address circuitry; this will determine where the exerciser begins generating data relative to the MUT start address. Two modes can be selected; either $VA = 0$ which starts data while the address of block is at zero, or $VA = \bar{0}$ in which the data start position is random. Both modes however, allow for selection of data starts in any of the 4 clocking phases between CCD clocking cycles.

The MUX Factor Select switch is used to hold each data bit for 1, 2, or 4 bit times to exercise each of the parallel paths in a multiplexed memory with the complete data pattern. The selection switch divides the frequency of the clock to the data generator by the MUX factor.

The choice of data pattern should then be made using the Data Source Selector. If the switch registers are chosen, and 16-bit repeating pattern can be set up. The Block Size should be set to correspond with

that of the MUT so that the block address code can be inserted into the data stream at the correct times if this option is selected. After determining the length of the data pattern required the Data Patterns Repeat Exponent should be set to obtain that length. The logic level on completion of that pattern must be set with the background switch. The tester data output can be complemented by selecting the DATA position of the DATA/DATA switch. Finally, the data output amplitude should be set. Once the controls on the front panel have been adjusted it is necessary to push the Reset button to ensure that variables set or changed on the front panel will be loaded into the exerciser circuits prior to starting the test.

By pressing the Start Test button the WRITE sequence begins. The exerciser system waits for the proper address location if the VA = 0 control is engaged, and the proper clocking phase prior to starting the data generator. Data will be generated until the data pattern repeats counter overflows. The data control circuitry then shuts off regardless of the state of the memory system.

When the End of Test light comes on the WRITE operation has been completed and the exerciser is in its quiescent state awaiting its next operation.

4.4.3 READ Mode Procedures

The anticipated data output of the MUT is generated within the memory exerciser for direct comparison with the actual data output. The front panel controls must be set up to generate this anticipated pattern. Since the background is not generated until the completion of the data pattern, the Background control has no effect on the test. The VA = 0/VA = $\overline{0}$ and Start Phase controls do not effect the test since these controls are activated only in WRITE mode. The clock frequency, amplitude, and pulse width may be varied within the limits of the memory exerciser. Finally the WRITE/READ switch should be in the READ position. Provided all these conditions are met the Reset is the last button to be pressed before the Start Test is activated. The exerciser is now primed and waiting for the Data Input Available signal to be asserted, thereby indicating that valid data is being presented at the Data Input terminal. Internally generated data and data from the MUT are presented simultaneously to the data comparator. Any deviation from the anticipated data output will be considered an error.

Errors are totaled and registered on a decimal display on the front panel. An error count is accumulated until the Data Input Available signal goes high or the Data Pattern Repeats counter overflows. Upon the completion of a test the error counter is disabled and the End of Test lamp comes on simultaneously with either the PASS or FAIL indicator.

4.5 Conclusions

The sole purpose of the memory exerciser is to adequately test the memory system attached to it. With the addition of a digital logic recorder it also becomes a versatile memory system debugging tool and an effective demonstration system. The logic recorder also permits the diagnosis of factors limiting the operating range as well as failure modes associated with the system design.

To this end the memory exerciser must be able to exercise both the actual memory of the system and the peripherals used to control that memory. The effectiveness of this type of testing depends on the operator to perform tests which localize the errors and vary the tests as necessary to determine the source of the errors.

V. SYSTEM TESTS

5.0 Introduction

A series of tests have been used to verify correct operation of the buffer memory system and to examine the system limits of operation. Debugging methods will not be discussed since debugging is here considered to refer to investigation procedures required to isolate and correct a fault that was found during testing. The only discussion of fault correction will concern necessary changes to the system due to hitherto unsuspected characteristics of the memory devices. Emphasis is placed on testing techniques suited to block-oriented random access memories which use shift register type devices. This chapter contains an outline of the tests that were performed and the results of those tests.

5.1 Test Plan

A testing program was devised to exercise the memory with a sufficient number of data test patterns to demonstrate that the memory is insensitive to the pattern of the data and to verify the integrity of memory locations; i.e., input data must be stored in specified locations and only in those locations. Data storage and retrieval also inherently test most of the memory, system logic controls. Limits of operations are studied by varying the CCD clock timing, the clocking frequency, the input clock pulse width, the input data and clock voltage levels, and the levels of the system power supplies.

5.1.1 Test Equipment

Several pieces of equipment were indispensable in carrying out the buffer memory system tests. The equipment included;

- (a) an oscilloscope - Tektronix model 7603, 4-trace oscilloscope,
 - (b) custom memory exerciser - described in chapter IV,
 - (c) pulse generator - 10 MHz. range,
- and (d) digital logic recorder - Biomation model 810-D

Triggering of the digital logic recorder could be made on any trace or any combination of the 8 traces. This feature enabled the tester to isolate any fault and observe the timing of test points both before and after the occurrence of the fault.

5.1.2 Memory System Functional Tests

The testing program and some of the rationale for the tests is given below.

1) WRITE/STORAGE/READ operations: A standard test pattern (see below) at a nominal 600 KHz data rate is used to check operation of all logic circuits involved in the WRITE mode of operation. The data stored in the WRITE operation is retained for a nominal period of time, e.g., 1 minute, and verified for retention by a READ operation clocked at 600 KHz. The readout is also used to check all logic involved in a READ operation.

2) Pattern sensitivity: The custom memory exerciser of chapter IV is capable of generating a large variety of data test patterns. Although additional patterns may be needed for debugging faults, the limited set of test patterns described below have been found to be well-suited to testing recirculating serial CCD shift register memories. The patterns are varied both in sequence and in length. The system was tested with each of the patterns described below and their compliments.

(a) Standard test pattern: (1011111101000000) repeated 2^n times, where n is an integer equal to or greater than zero. Any pattern that repeats in integral number of times within a CCD track recirculation or a memory block length makes for easy observation on an oscilloscope because of the ease of oscilloscope triggering. Although the oscilloscope trace is useful as a first indication that the memory system shows signs of correct functioning, the results may be misleading. For example, a single bit error within a memory block may not be observable on the oscilloscope since the trace trigger may not show the particular repeat of the test pattern which contains the fault. However, the custom memory exerciser has been designed to read out the total number of data bits in error during a memory system readout operation. Therefore,

even single errors in any test run can be detected. By triggering on the tester error signal, the digital logic recorder can be used to analyze the fault condition.

Since the CCD storage medium is a recirculating shift register, all memory storage locations within a track are exercised with each data bit. Therefore, testing routines that have been designed for RAM's may not be suitable for CCD's. The standard test pattern described here gives a strong indication of correct CCD performance. If the memory exerciser is set to MUX = 4, then each CCD will receive the complete data pattern. Then, each storage location is exercised both with a 0 following a string of 1's and with a 1 following a string of 0's. The pattern also contains single "01" and "10" combinations.

Since each data bit exercises each storage location within a track, a more severe test is to demonstrate that a stored 1 can be overwritten by a 0, and a stored 0 can be overwritten by a 1. This test is easily accomplished by first storing the standard test pattern into any memory block. Then the block flag for that block is cleared. Since the CCD clock rate is never reduced below the minimum transfer rate for the CCD's, data in the CCD's are never destroyed by a destructive readout or a block flag clearing operation. Then, the compliment of the standard test pattern is entered, thereby overwriting each previously stored data bit with its compliment.

A second manipulation of the standard test pattern is used to exercise another critical point in the CCD operation, particularly if the data outputs of the CCD's are wire-OR'ed, as is the case with the buffer memory. It is important to exercise the last data bit in the last memory block to be accessed in one memory bank and the first bit in the first memory block to be accessed in another memory block with all combinations of data bits, i.e., 00, 01, 11, and 10. It is at this point when the CE signals to the chips in each memory bank switch state. This test is easily accomplished by ensuring that the number of data patterns repeat exponent on the memory exerciser is large enough to make the pattern length great enough to test contiguous memory banks. Then

the WRITE, idle, READ tests are repeated with the standard pattern (1011111101000000), its compliment (0100000010111111), a shifted standard pattern (0101111101000000), and the compliment of the shifted pattern (1010000001011111). Since an integral number of these patterns is contained within a memory block, the last bit of the pattern is the last bit in a memory block, and the first bit will be the first bit in the next memory block.

(b) Single bit pattern (00000000000000010): Although this pattern could be used to perform similar tests to the standard test pattern, the single bit pattern can be used both to check crosstalk and to demonstrate the storage of only 1 bit when the rest of the memory contains its compliment. First, the entire memory is filled with 0's. Then, the exerciser's number of patterns repeat exponent is set to 0, and the background bit is set to 0. The block flag of any memory block is cleared and the test pattern is entered. Then, the entire memory is checked to ensure that the only "1" bit is located in the proper position in the accessed memory block. All other bits in every memory block must remain 0. The compliment of this test should also be performed.

(c) Pseudo-random pattern: Pseudo-random data, whose pattern varies according to the pre-determined data length, is used to more closely simulate real operating conditions than do repeating patterns.

3) Test data length: The memory system has been designed to accept any length data stream up to the available memory capacity. Any of the test patterns described above could be used. Since the memory structure uses 4 tracks of each CCD group for a block, a complete CCD group (8 blocks) for a memory bank, and 4 banks for the system, a suitable set of test data lengths would be;

- (a) less than $\frac{1}{4}$ block length, say, one 16-bit pattern
- (b) exactly $\frac{1}{4}$ block length,
- (c) $\frac{1}{2}$ block,
- (d) 1 block,
- (e) 2 blocks,
- (f) 8 blocks (1 bank),

- (g) 2 banks,
- (h) 4 banks,
- and (i) more than 4 banks to exceed memory capacity.

Test data length of less than 1 block is required to check transfer timing logic to ensure only integral block length transfers are made. Similarly, integral block lengths are needed in the test to ensure that 1 data block is stored in precisely 1 memory block, with no under or overflows. The overflow indicator and transfer halt logic is tested by using data lengths equal to or greater than the available memory capacity.

4) Memory integrity: Tests must be performed to ensure that all input data is stored in the assigned memory locations and only in those locations. Three techniques were used.

(a) The custom memory exerciser was designed to permit a unique address code to be inserted as part of the data stream for each memory block. The address code contains chip enable and block, in bank code information. Readout of each memory block in turn is monitored with the digital logic recorder to capture the beginning of each memory block transfer. A check of the address codes in the data stream verifies the uniqueness of each memory block and the correct functioning of the address logic.

(b) The test involving the single bit pattern as described above is also a check for memory integrity.

(c) If a pseudo-random pattern whose length is equal to the total memory capacity is used, then every memory block will be filled with a different pattern. Such a test confirms the uniqueness of the memory blocks.

5) Block and Bank Access: The block selection controls must be exercised in a number of ways. Some of the tests described below are performed inherently in the above tests. The system provides the option for automatic or manual selection of access to the memory blocks.

In AUTO mode;

(a) set data pattern length equal to 1 block, repeatedly request WRITE transfer until the memory system is full. With each access, the next empty location, regardless of the states of the individual block selection switches, should be filled.

- (b) repeat (a) with data pattern length less than 1 block,
- (c) repeat (a) with data pattern length greater than 1 block,
- (d) clear some of the memory block flags in each bank and repeat tests (a) to (c),
- (e) WRITE into a single block, then READ,
- (f) WRITE into several contiguous blocks, up to full memory, then READ,
- (g) WRITE into several blocks, clear some of the block flags, then READ. In each of these tests, all blocks whose flags are set, should have been accessed in turn. The digital logic recorder is useful in this test if the CE and track addresses are monitored.

In MANUAL mode,

- (a) all of the tests in AUTO mode are repeated, except access to the blocks is controlled manually in sets of 1 block, several blocks that are not necessarily contiguous, 1 bank, several banks, or full memory,
- (b) WRITE into a block in 1 bank, verify that data has been stored correctly; WRITE into a block in another bank and verify. Again verify the data in the first block, and then again in the second block. This test is needed to verify that access to any block during one transfer does not affect data stored during a previous transfer.

In both AUTO and MANUAL mode, check that any set of block flags may be cleared manually. The overflow monitor is also involved in controlling memory access. In MANUAL mode, if there are no empty blocks that have been selected, even though the memory is not full, input data should not be accepted. As soon as even 1 empty block becomes available, by manual selection of an empty block, by clearing the flag of a selected block, or by a destructive readout, the memory overflow monitor should reset.

6) Readout Controls: Two methods of data retrieval are permitted, destructive readout and non-destructive readout. The test of these controls could be performed during the course of the block and bank access tests. A check should be made in the non-destructive readout mode that the block flags remain set after the data transfer. In

the destructive mode, each flag for a block that has been accessed will reset. During a non-destructive readout test, if the memory overflow monitor was on before access, the monitor should go off during the readout and be re-asserted at the end of the data transfer.

7) Input Data Synchronizing Controls: The buffer memory system must be tested to ensure that it can accept incoming data beginning with any input clock pulse, regardless of position relative to the CCD start address or the CCD timing chain trigger interval. However, input data will be lost if the data input starts during a READ operation. The custom memory exerciser has the capability of initiating the test data stream during any preselected CCD virtual address and during any input clocking interval between CCD T.C. trigger pulses, which are denoted on the memory exerciser as start phases $\emptyset 0$, $\emptyset 1$, $\emptyset 2$, or $\emptyset 3$. It is particularly important to test the system with input data that begins while the VA = 0 signal is asserted, since this signal is involved in a great proportion of the system timing controls. Testing is adequate if the start of data location test is repeated for each of the 4 input clock phases during CCD virtual addresses 255, 0, and 1. Timing controls operate identically for start points in all CCD virtual address locations other than VA = 0.

5.1.3 System Limitations Tests

The system limitations are defined by the upper and lower limits of data access frequencies, the clock and data levels, and the power supply range that permits operation over the specified frequency range. Each of the parameters which affect the limitations listed above should be adjusted to determine system performance capabilities.

(a) Data access frequencies: The data access frequency limitations are defined by the CCD clock timing, the timing chain trigger frequency, the timing chain trigger pulse width, and the RAM WE pulse width. Each of the pulse widths should be reduced to the minimum width that will permit system operation at the nominal CCD power supply operating point of $V_{DD} = +10$ VDC and $V_{BB} = -3$ VDC. Since the $\emptyset 3$ clock pulse width varies according to clocking frequency, the minimum $\emptyset 3$ width will determine the maximum trigger frequency. The minimum frequency will be determined either by the CCD refresh timing interval requirement or the idle frequency controls.

(b) Data and clock levels: Since the system inputs are required to be TTL compatible, the system should be tested with data and clocking logic ONE levels at both 2.4V and 5.0V. The input clock pulse width may also be varied to determine its limits.

(c) Power supply range: After satisfactory system performance has been achieved at the nominal CCD operating point, $V_{DD} = +10V$, $V_{BB} = -3V$, each of the power supplies are adjusted until system errors appear. A suitable test pattern for this test is a pseudo-random pattern of full memory capacity test. A range plot, sometimes called a Schmo plot, can be drawn to show the range of operation.

5.2 Test Results

5.2.1 Memory System Functional Test Results

Each of the functional tests was performed on the memory system. Although a number of faults were detected with these tests, the faults have all been isolated and corrected. At a nominal 600 KHz input clock frequency, with all inputs at standard TTL logic levels, and with $V_{DD} = +10V$, $V_{CC} = +5V$, and $V_{BB} = -3V$, the system now passes all the functional tests. Both WRITE and READ operations have been verified. Data has been retained in the idle mode during a 24 hour test. All test data, regardless of pattern or length, can be stored and retrieved from the memory system. Memory integrity has been verified by using the block address code insertion into the data pattern, by the single bit pattern, and by the pseudo-random pattern test. All memory blocks can be accessed individually or in ordered sets. Access can be made either in AUTO or MANUAL select mode. Both destructive and non-destructive readout operations can be performed. It has been verified that incoming data can be accepted at any time without loss of any bits unless the data begins during a READ operation. Only data that arrives during idle mode or at the end of the READ cycle will be retained. A READ request that is initiated during a WRITE operation does not affect incoming data.

5.2.2 System Limitation Test Results

When the CCD clock timing parameters and the RAM WE pulse were adjusted to the minimum values as listed in Table 5-1, the system could be operated

with clock rates from approximately 120 KHz to 4.25 MHz. To allow operating tolerances, the memory system frequency range is specified to be 150 KHz to 4.0 MHz. The input clock pulse is required to be a minimum of 35 nsec. wide to operate the system.

<u>Timing Parameter*</u>	<u>Minimum Timing (nsec.)</u>
T.C. Trigger ($\phi 3$ - $\phi 2$ reset)	160
$\phi 2$	330
$\phi 2$ - $\overline{\phi 1}$ overlap	100
$\overline{\phi 1}$	135
$\overline{\phi 1}$ - $\phi 2$ overlap	95
$\phi 3$ delay	290
$\phi 3$	130
RAM WE pulse (LO true)	180

*See Appendix A for timing diagram

Table 5-1 Minimum Timing Parameters

All system inputs were demonstrated to accept TTL logic levels. The range of system operation as a function of both CCD power supplies and frequency is shown in Fig. 5-1. Some evidence was uncovered during debugging indicated that the upper frequency limit was caused by the RAM frequency limit, rather than the CCD's. A READ operation was successful at over 4.5 MHz. Although the system will operate with lower power dissipation at $V_{DD} = +10V$ and $V_{BB} = -3V$, the tolerance allowable on the power supplies was found to be relatively small. Wider operating margins, at the cost of greater power dissipation, are possible if $V_{DD} = +12V$ and $V_{BB} = -5V$ are selected as the supply voltages.

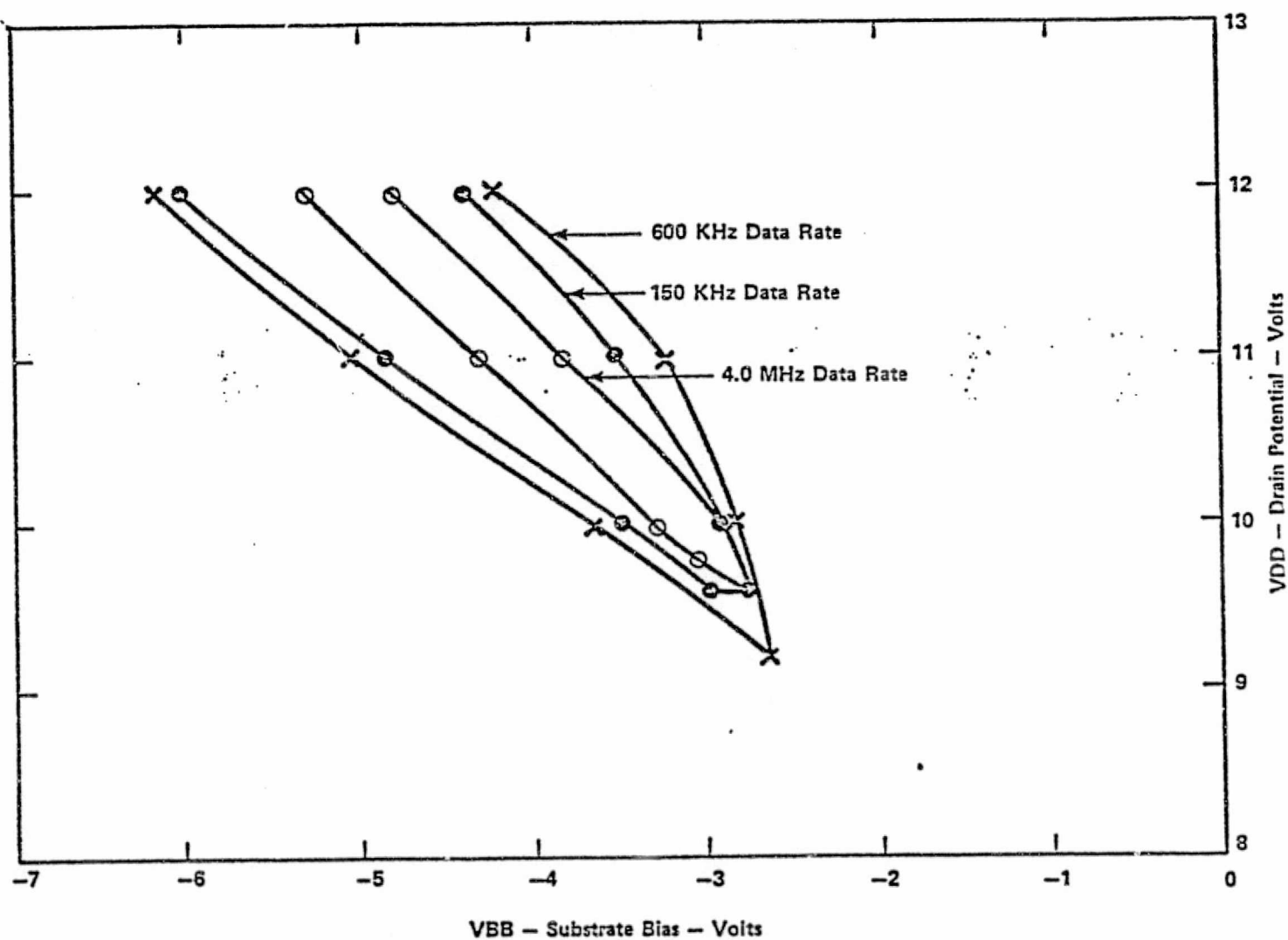


Figure 5-1 Range Plot For 128 K-Bit Buffer Memory System

5.2.3 Additional Comments on CCD Performance

In the course of system testing and debugging, a number of unsuspected characteristics of the CCD memory chips were uncovered.

1) The memory system was originally designed to keep the CCD clock level static to those memory banks which did not contain active blocks. The clocks would be maintained at those levels needed to keep driver dissipation low, i.e., the $\phi 1$ and $\phi 3$ clocks would be kept high. The power supply to the $\phi 2$ driver, whose output would have to be in the normally high-dissipation, low output state, could be gated to conserve power. However, it was found that the CCD's would not accept input data reliably unless they were clocked for nearly one shift register recirculation, that is, 256 transfers. Hence, all memory banks, whether actively retaining data or not, are clocked at 15 KHz \pm 3 KHz during the idle state.

In a memory system redesign, the clocks could be controlled to start 1 recirculation before a data transfer. Since the $\phi 1$ and $\phi 3$ drivers have such low duty cycles in the idle mode, there would be no significant power saving by switching to a static mode. Only if power supply gating to the $\phi 2$ drivers were implemented would there be a driver power dissipation saving. However, a speed penalty would probably be incurred unless the power supply gating - which in itself must operate with less power than the power to be saved - must be able to supply the large charging current required for $\phi 2$ operation. The system clocking is presently tuned for 4 MHz operation. If the power supply gating is inefficient, the rise and fall times of the $\phi 2$ clock output are increased, thereby reducing the maximum system clocking rate.

2) In the initial design, the $\phi 3$ clock input to the CCD was also tied to the CCD pin 8 (sense amp data output) to achieve an on-chip data sample and hold. This would save an external data buffer register. For a single CCD memory this feature works properly. However, if the data outputs of several devices are wire-ORed, then if the last output

bit from one device is LOW (and CE is inhibited) then the output node remains LOW and will not recover for several clocking intervals, thereby possibly causing errors in the data outputs from other devices. This fault was corrected by tying the pin 8 of each CCD to V_{DD} instead of $\phi 3$. The output node then recovers at the beginning of the next $\phi 2$ interval. Since data is no longer maintained with an internal sample and hold, and external data buffer has been added. Output data is strobed into the buffer approximately 150 nsec. after the rise of $\phi 3$. This solution also overcame the CCD characteristic that is described below.

3) In most memory systems, the $\phi 3$ clock could be expected to operate with a fixed pulse width. Since power consumption in a clock driver is reduced when the driver output is high, the $\phi 3$ clocks in the buffer memory system were designed to have a variable pulse width. As the system frequency is reduced, the $\phi 3$ pulse width stretches. Output data is specified to be valid till the end of the $\phi 3$ clocking period. However, it was found that the data output from some devices reverted to the HIGH state after a few microseconds. This phenomenon appears to be related to the track used to store data and to the proximity of the power supply operating point to the edge of the CCD range of operation curve. There would be no error at high frequencies or if the data output would normally be HIGH. This condition was easily overcome by the extra data output buffer mentioned above.

VI. FURTHER DEVELOPMENT

6.0 Introduction

The current feasibility design has demonstrated that CCD's can be applied advantageously to the problem of low power digital storage and particularly to the problem of interfacing widely varying data rates. Undoubtedly much of the benefit related to using CCD's as opposed even to devices such as a low power RAM lies in the amount of data that can be stored that does not require direct interaction with on-chip or off-chip peripheral circuitry. Each stored bit of RAM must be fetched by addressing its location via peripheral circuitry, whereas the data stored in each CCD block automatically arrives at the output port without any direct action other than clocking being required. Storage is affected in a similar fashion. Therefore a simple counter with no direct interaction with the CCD's is sufficient to supervise the location of all bits within a data block.

Mass or "bulk" data storage is presently generally configured in serial form and usually comprises magnetic media, namely disc or tape. Each of these place limitations in terms of access speed, data bandwidth capability, and power, these systems being electromechanical in operation. Magnetic bubble memory overcomes the latter objection but still presents bandwidth and access speed limitations. Therefore, any consideration of CCD's as a memory medium must take into account the total system objectives. It is feasible to consider a bulk memory consisting either totally of CCD memory or alternately consisting of a combination of two media, such as CCD and magnetic bubble, or CCD and RAM, to combine speed with low power as in the system herein described.

It is apparent that the present study and prototype system is centered around relatively long term storage of sequentially arriving data, in fact a data recorder, and that continuous high speed access or high speed recovery of stored data is not the highest priority. Therefore, a combination of two storage media in an optimized fashion is economically sound. There are a number of options to be considered when accessing future system architectures:

- (1) utilization of the present memory device or its direct successor, and optimizing the system architecture,
- (2) utilizing the latest advances in CCD memory device design,
- or (3) configuring a specific device architecture to optimize the system design.

Each of the options will be evaluated in discussions concerning both expanded versions of the prototype buffer memory system and related CCD memory system architectures.

5.1 Further Development of Present Buffer Memory Configuration

The present memory system is a prototype feasibility model of limited memory capacity and contains features that can either be simplified or augmented in a future CCD memory system. A larger system of the same form with a capacity of, say, 1 M-bit to 10 M-bits is considered to be feasible. Here a number of options which can be made in an expansion of the present memory configuration are discussed.

The current design provides for access to any ordered set of memory blocks within the 32 available. Completely random access to the blocks can be made only by successive transfer requests to individual data blocks. Some time to set up the request and address synchronization is needed between transfers. Although this limitation is probably not serious in the readout mode, it could be detrimental to storage of a long data input stream. It is recommended that an expanded memory system be based on computer control, both to provide complete randomness of data block selection and to optimize the peripheral hardware. The hardware that is presently used to identify and control blocks in use and address decoding logic would then be completely eliminated. The system, presuming the same general specifications concerning data rate, etc., would then reduce to the clock drive circuits, the storage devices, the output buffer, and the input pre-buffer comprising the high-speed RAM's. This represents a tremendous simplification in memory system hardware and for any expanded system

must be considered essential to the economic viability of such a buffer memory system. The use of high speed bipolar microprocessors, or perhaps even existing MOS microprocessors of the 8080A variety would permit control of a memory system orders of magnitude larger than the present model. Possibly this would render the use of a different memory medium such as magnetic bubbles for the long term storage less attractive than would at first appear. Conversely present day microprocessors conceivably have the speed and power to affect control over a complete dual media memory system.

Assuming sequentially arriving data streams at varying data rates, the requirement to capture and store these "blocks" of information for subsequent use or transmission would be met by the identification by the microprocessor of an available memory block. The block size can change from the present 4K size. With the existing configuration which uses 8K CCD's and 4-way multiplexing, the block size can vary from 1K to 32K. The microprocessor would store the status of the data blocks and, if necessary, some pertinent information relating to the material content of each data block so that recall can be affected, under program control, according to the type of information required, the data source, or even the time of data capture. A substantial portion of the input pre-buffer, such as the RAM buffer, could be eliminated if the microprocessor were to store the CCD virtual address concurrent with the start of the block transfer. There would be no need to wait for the CCD zero virtual address before starting the CCD input transfer. Output transfers would begin when the block virtual address matched the stored start address.

For a large system, expansion should be by duplication of the basic memory module - including clock controls and virtual address circuitry - rather than by simply expanding the number of banks in a system. This is necessary to maintain minimum power dissipation since all non-accessed banks in the memory module are called upon to operate at one quarter of the clock frequency of any bank that is accessed; this obviously increases the power drain at higher clock rates. Allowing duplicated complete subsystems to remain at idle rate while data is being transferred in or out of an accessed

bank in one subsystem ensures minimum power dissipation. It may also be noted that peripheral hardware does not increase proportionally to increased memory capacity. Therefore, in a large memory system, particularly one that is partitioned into several memory modules, the average power dissipation per bit is reduced substantially both in idle and transfer modes.

No mention has yet been made of the possibility of providing parallel data streams. Duplication in a parallel fashion of the subsystem as described above can provide multiple channel parallel data transfer into and out of the memory. Under program control, the system could handle either single channel serial data or parallel format word transfers. Thus, 8 subsystems in parallel would permit a maximum of 32 M-bits/second data transfer rate.

5.2 Application of Advanced CCD Memory Device Configurations

It now remains to examine the potential of different CCD memory device configurations to the application of expanded memory systems. The present BNR CCD memory device organization is in many respects particularly suited to the application. Considering low power in the "idle" mode to be the highest priority then the refresh of data within the device every 32 clock pulses permits extremely low clock frequencies to be used with a consequent power benefit. Any dynamic semiconductor has an inherent storage period without refresh of approximately 2 msec. at room temperature. This figure is determined by allowing between one and two orders of magnitude margin for dark current saturation, thus most devices will retain data for 50 to 200 msecs. before false data bits are detected. By refreshing data more frequently (i.e. fewer clock cycles between refresh) on the device an overall lower idle power is required. It is feasible to consider 16K CCD's of the same organization, and indeed there is in the market now a device very similar in organization to the BNR device, the Intel 2316 16K bit CCD. However, this device is not as simple to use and requires extensive peripheral circuitry, thus detracting from the appeal of its potential low power performance. It would be quite feasible to modify the present 8K design to reduce the size and increase the total storage to 16K bits at the same time retaining the inherent low power operation consistent with the basic 32 bit between refresh mode.

Long term retention of data with the present system represents no problem and it can easily be shown that much of the circuitry presently devoted to control during idle operation can be fabricated in custom CMOS, thereby drawing negligible system power. Circuit developments in industry have now produced clock drivers with low D.C. power dissipation leaving the fundamental CV^2f product as the prime power dissipation component.

Computer memory systems have one overriding criterion, they must cost as little as possible. Thus CCD memory device design has concentrated on maximizing density and secondarily providing higher operating speeds and low power. A new architecture recently proposed and developed by Bell-Northern Research uses a form of data multiplexing to increase the memory density while at the same time making on-chip drive of that memory feasible. This is the serial-parallel-serial (SPS) structure described in Appendix G. One drawback of this design in the present system context is the reduction in dynamic range of data rates which can be handled. Whereas the 8K CCD was optimum from the point of view of offering at least a two decade range of data rates, this is not possible with the SPS structure. The two limitations are:

(1) Upper data rate.

The speed with which a CCD shift register will run and the clock power required to drive it at that speed.

(2) Lower data rate.

The time for which data is stored on chip between refresh.

With the 16K CCD, the input and output high speed shift registers (presently specified at 10 MHz) place the limitation on the upper data rate, whereas the bulk memory array size determines the limitation of the lower data rate. (The 16K CCD having 4K bits of storage in the bulk means a nominal 2 MHz lower data rate for 2 msec. storage time. Actually the device is specified at 1 MHz permitting 4 msec. data storage.) Reducing the number of the storage elements between refresh would improve this range down to the present 8K with 32 bits between refresh which allows approximately 10 KHz as a lower data rate.

However, there is of course a penalty in terms of area per bit due to the increased number of refresh amplifiers required by the 8K CCD.

Implementation of a buffer memory using the 16K CCD can be accomplished with substantial improvement in overall performance. An upper frequency limit of the data rate, 5 MHz, can easily be met by direct interfacing of the CCD memory device. The time taken for the memory to recirculate at high speed is 400 μ sec. This, therefore, is the worst case delay for which arriving data would require buffering before being written into the CCD memory. Thus a simple, small serial buffer is all that is required to interface a low speed data stream to the storage device. Various multiplexing schemes are feasible using this device to both increase the high data rate or reduce the lower data rate consistent with low power operation of the device.

If the requirement is restricted to capture of high speed data and recall of that data subsequently at that data rate or lower (say down to 150 KHz for bubble memory compatibility), then a simplified design will suffice with two shift registers; one for data storage, and the second taking data from the first for output buffering. Each shift register has separate clocking.

In the present 16K CCD organization, each device has four inputs and four outputs, therefore by using a four bit buffer a data rate of up to 40 KHz could be captured in one device. If this is not a desirable feature then possibly either a simple modification of the design to permit only a single input and output or the provision of a two bit address and control of individual 4K block write/recirculate lines may be preferred. A redesign of the present 16K could also dramatically reduce the present quiescent power dissipation which is due to a number of timing overlaps on dynamic gates. Present day technology can achieve smaller 16K designs or 64K designs, thereby again reducing the operating power per bit associated with the bulk memory CV^2f product and the overhead D.C. power dissipation.

The design of a 1 - 10M bit memory buffer could be implemented equally well either using the present 8K CCD organization or the very different 16K CCD organization. The trade-off is between data bandwidth range and low idle power. Low idle power becomes a problem only if the CCD is the only memory medium being used. If non-volatile memory such as bubble is to be used for the longer term (minutes and hours), then low power during capture and transfer is more important because the CCD memory will become inoperative for the majority of the time, thereby having close to zero dissipation.

5.3 Other CCD Memory System Configurations

Alternate memory system configurations can be suggested from the feasibility model. Rather than a system expansion, a relatively simple data recorder can be envisioned. A minimum block size of 1K-bits with purely sequential block access can be used as a tape recorder replacement. If some data loss can be tolerated either at the beginning or end of a transmission - such as with a tape recorder - no complex data synchronizing logic is required. If the data bandwidth were restricted to 10 KHz to 1 MHz, then no data multiplexing or idle control circuitry is needed. Only CCD clocking logic, virtual address counter, and an address pointer is needed. In this frequency range, the 8K CCD or an expanded 16K device could be used with a minimum block size of 256 bits. The amount of data lost at either end of a transmission is reduced by having a small block size.

If the data recorder application called for higher data rate capture and a larger storage capacity, the SPS memory structure with 4K-bit blocks would probably be more feasible. Proposals are in hand to examine and design a 64K-bit high density CCD memory using an organization very similar to the present 16K CCD. It is expected that such a device would exhibit less than 5 μ W/bit power dissipation at high speed operation and less than $\frac{1}{2}$ μ W/bit at low data rates. Special consideration would be given to widening the data bandwidth and reducing idle power by suitable re-organization of the fundamental memory block size - presently 2K-bits. This could be reduced to 1K-bit. Access time could be improved and both idle power and speed reduced.

It is necessary to consider each system requirement in detail before arriving at any decision regarding the storage device. Consider an application requiring capture and storage of very low speed data, say <1 KHz. Two implementations will be discussed.

(a) Use of BNR 8K CCD.

The use of the present 8K CCD or a redesigned 16K CCD retaining the same configuration can be achieved with the memory cycling continuously at the low power or idle rate, say 10 KHz clock rate. Thus with a 256 bit register the time for all registers to recirculate is nominally 25 msecs. Therefore a maximum of 25 data bits can arrive in the recirculation interval. Two 25 bit data buffers are then required to interface incoming data with the appropriate timing and control logic to route the output of each shift register alternately to the correct register and location within each register of the CCD memory bank.

(b) Use of 16K SPS Memory.

If the lower clock rate of this device is nominally 1 MHz, then a maximum of four data bits can be buffered during the recirculation time within the 4K sections which make up the 16K. Thus, a four bit parallel input into any selected 16K device can be effected when the 4 bit input buffer becomes full. Due to the greatly reduced input clock capacitance of this device compared to the 8K CCD, low power CMOS drivers can be used thus maintaining total system power below 1 μ watt/bit.

5.4 Conclusions

A number of possible CCD memory system developments have been suggested. It is apparent that the capacity of a CCD system could be expanded by orders of magnitude with a substantial reduction in the power dissipation per bit. The data bandwidth capability could be extended upwards by increased levels of multiplexing or by providing for parallel data I/O. A modification of the input buffer would extend the lower frequency limit to any arbitrary value. The most beneficial near-term solution to the problem of optimum low

cost, low power, wide bandwidth data recording for airborne or satellite use is judged to be an extension of the basic principles demonstrated in the assembled feasibility system. However, the optimum device configuration relating peripheral circuit area to storage area is met using the 4K-block size on the SPS structure. Therefore, it is recommended that further developments incorporate devices similar to the BNR 16K CCD to yield flexible, self-contained data recorder systems.

APPENDICES

A P P E N D I X A

8K CCD Specifications



CC8M03 8192 - BIT CCD DECODED MEMORY CHIP - PRELIMINARY DATA

CHIP n-channel CCD, dimensions 178 x 168 mils

ORGANIZATION 32 tracks (loops), 256 serial bits per track;
random access to any track within one bit-time.

INPUT/OUTPUT Sequential Read/Write during single bit-time; output
occurs within one bit-time of applying address. Input
data replaces the data which was read out during the
previous clock period.

PACKAGE 22-pin dual-in-line; 16 active terminals, (see Figure 1).

and clocks: ϕ_1 , ϕ_2 , ϕ_3

TERMINALS d.c.: GND, V_{DD} , V_{BB}
control: CE (chip enable); A₁ to A₅ (track address);
W (write).
data: DI (input), DO (output for sense amplifiers), \overline{DO}
(output for TTL).

TIMING DIAGRAM Output data becomes valid during ϕ_3 high level while CE
(see Figure 2) is high; state of W has no influence on output. Input
data must be applied during ϕ_2 high level, and must be
maintained until after ϕ_2 goes low. The states of CE
and of the address decoder outputs are sampled on-chip
during ϕ_3 high level for control of writing during ϕ_2
high level if W is high at that time. Therefore, input
data always replaces the data read out during the previous
 ϕ_3 high level, even if the address has changed and/or CE
has gone low. This permits the swapping or modification
of complete blocks of data without any unproductive clock
periods.

OPERATING CONDITIONS Voltages are relative to GND.
 V_{DD} : 8 to 14 volts, V_{BB} : -1 to -7 volts.
CLOCKS, CE, ADDRESS, W: HIGH level = $V_{DD} \pm 1$ volt
LOW level = 0 to 0.8 volts
(CE HIGH level may be as low as $V_{DD} - 3$ volts)
data input: HIGH level = 4 to 14 volts
LOW level = 0 to 0.8 volts

CHARACTERISTICS	<p>DATA OUT to sense amplifier:</p> <p>HIGH level: 2 mA minimum into 100 ohms to ground</p> <p>LOW level : 10μA maximum into 100 ohms to ground</p>
	<hr/> <p>DATA OUT to TTL:</p> <p>HIGH level: equals external pull-up voltage</p> <p>LOW level : 0.4V maximum when driving one worst-case TTL load in parallel with 3 kilohm pull-up resistors; (connect pin 8 to V_{DD} to enable DATA OUT)</p>
CAPACITANCES	<p>ϕ_1 and ϕ_2 lines: each 700 pf maximum under worst-case conditions;</p> <p>ϕ_3 line: 150 pf maximum;</p> <p>ADDRESS lines: each 5 pf maximum;</p> <p>CE line: each 10 pf maximum;</p> <p>\bar{W}, DATA IN lines: each 3 pf maximum;</p> <p>DATA OUT, DATA OUT lines: each 3 pf when CE is LOW</p>
DC CURRENT DRAIN	<p>V_{DD} line 3 mA maximum, (CE HIGH); 6 mA maximum, during ϕ_3 HIGH level (CE HIGH); 1 mA maximum (CE LOW)</p> <p>ϕ_3 line: 2 mA maximum (CE HIGH only) during ϕ_3 HIGH level. No other significant d.c. current drain.</p>
NOTE	<p>Address HIGH level may be reduced to 5 volts for lower power operation with some reduction in operating range and performance.</p>

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OPERATING CHARACTERISTICS

PARAMETER	HIGH	LOW
V_{DD}	8 to 14 volts	
V_{BB}		-1 to 7 volts
clocks, A_1 to A_5 , CE, W	$V_{DD} \pm 1$ volt	0 to 0.8 volts
Data Input	4 to 14 volts	0 to 0.8 volts
Data Output - Sense amp	2 mA @ $R_L = 100\Omega$	10 μ A @ $R_L = 100\Omega$
Data Output - TTL	EXTERNAL PULLUP	0.4 volts

PARAMETER	TIME (ns)		
	MIN	TYP	MAX
t_1 ϕ_1 clock low level duration	90		
t_2 ϕ_2 set-up time	100		
t_T ϕ_1 or ϕ_2 clock transition time	25		
t_3 ϕ_3 width	100		
t_{OV} overlap time between ϕ_1 and ϕ_2 high levels	0		
t_C decode time	140		
t_L input lead time	100		
t_W write command hold time	80		
t_H data input hold time	50		
t_{D1} data output delay time (pin 8)		50	
t_{D2} data output delay time (pin 7)		80	

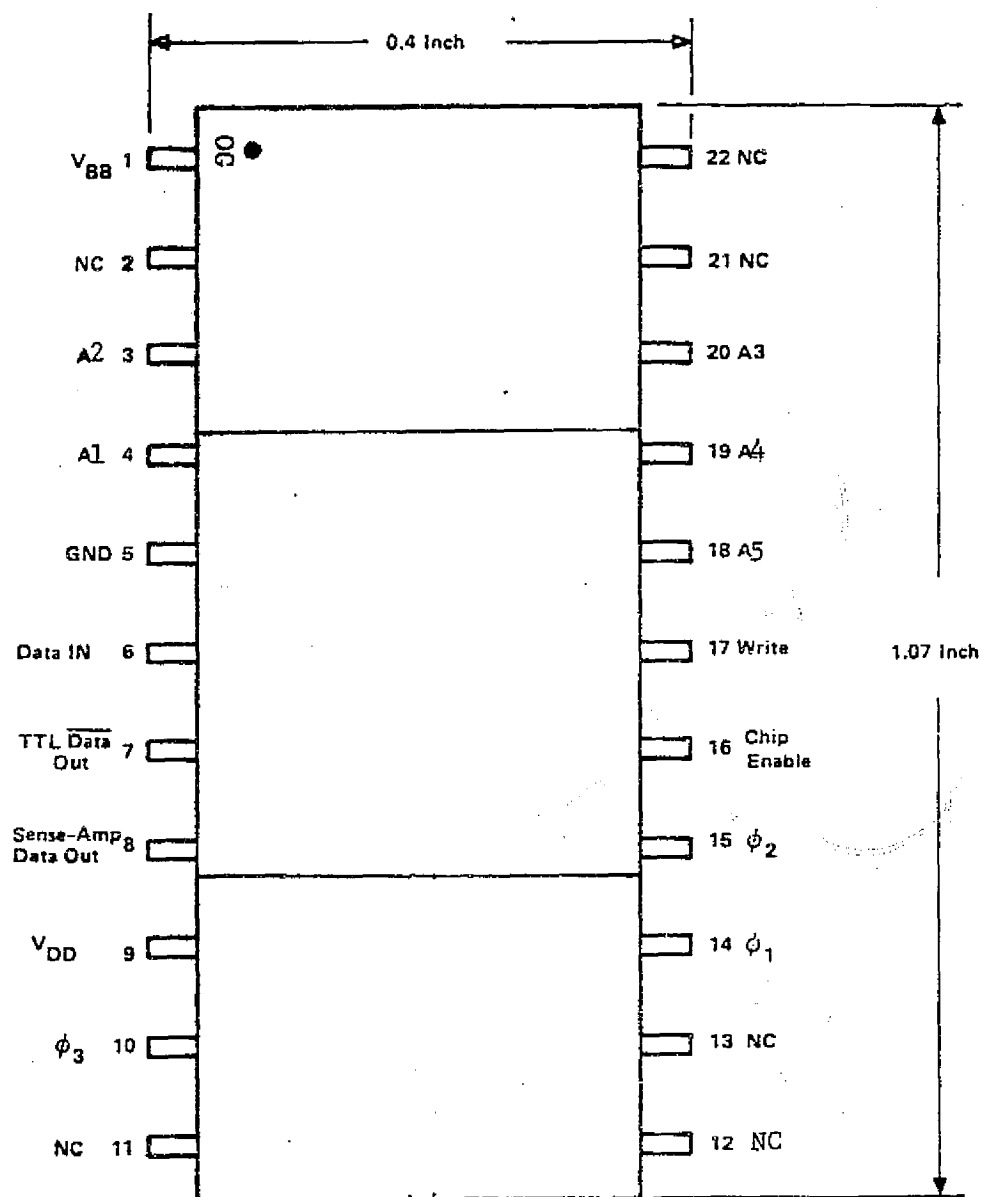


FIGURE 1
Package and Pin Connections

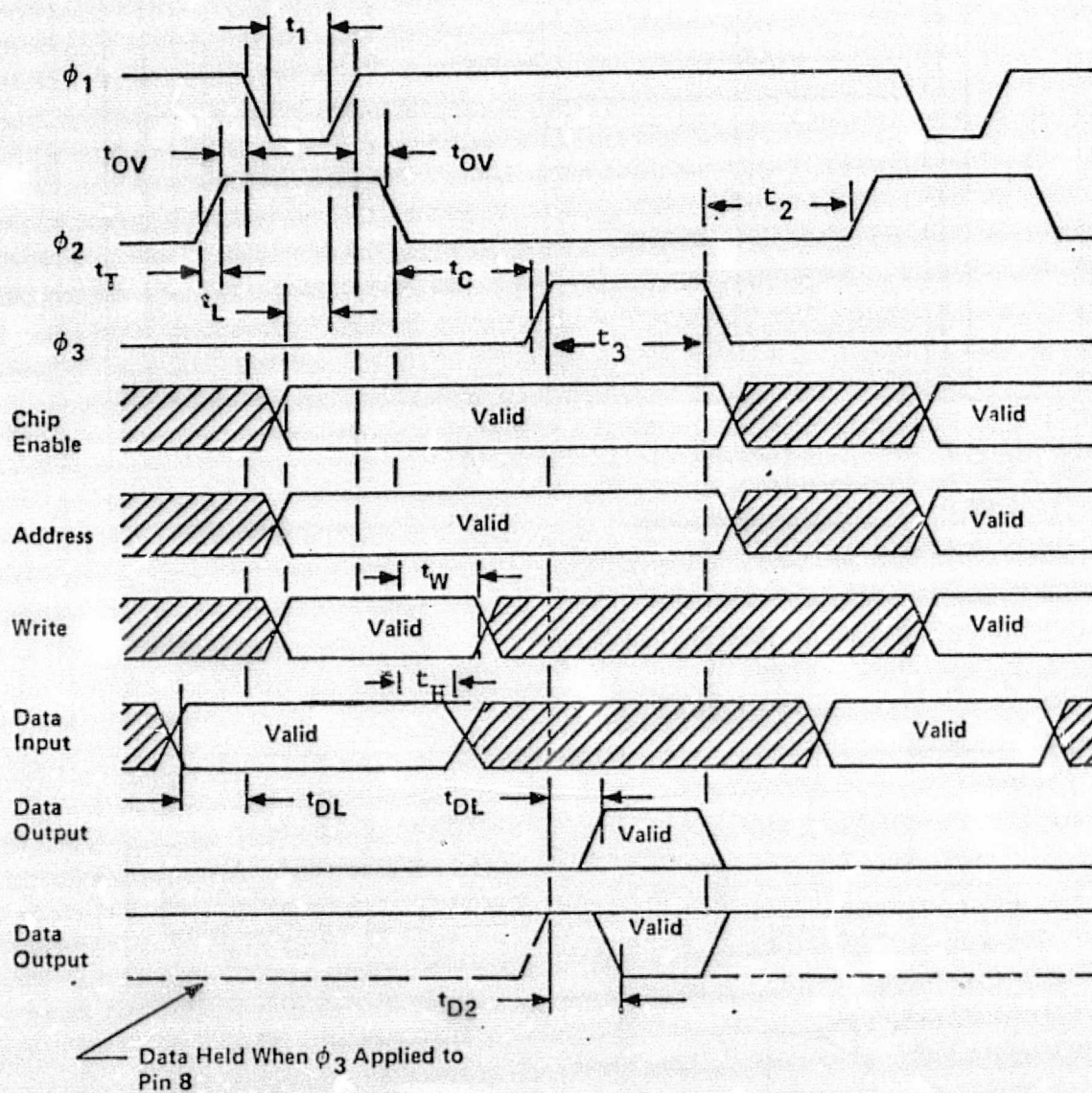
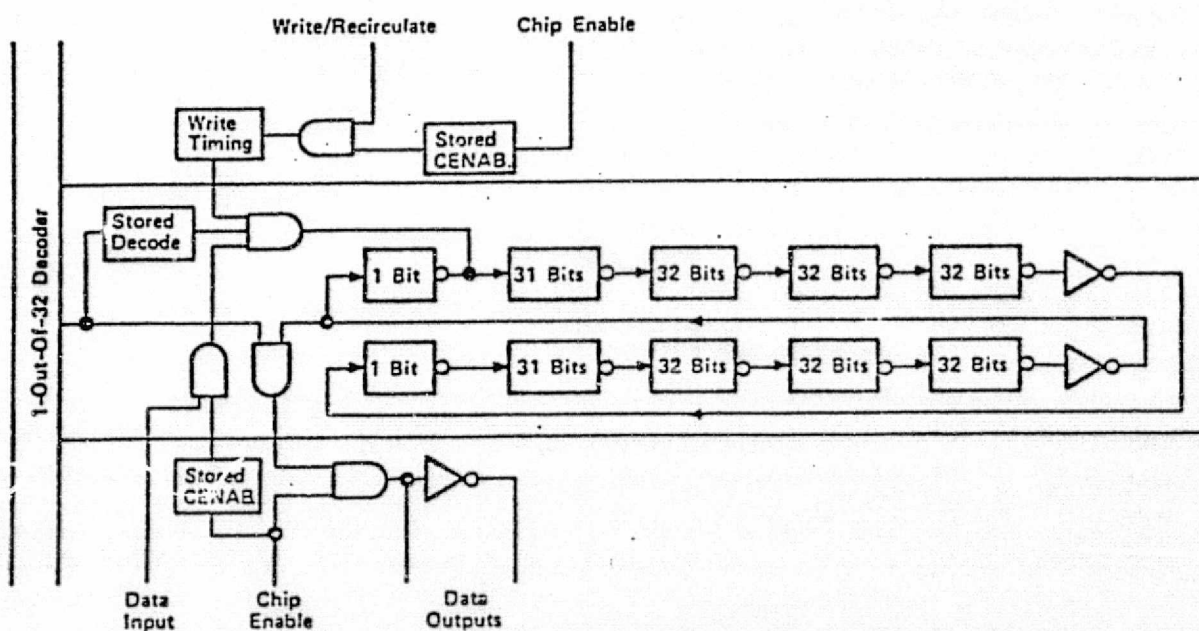
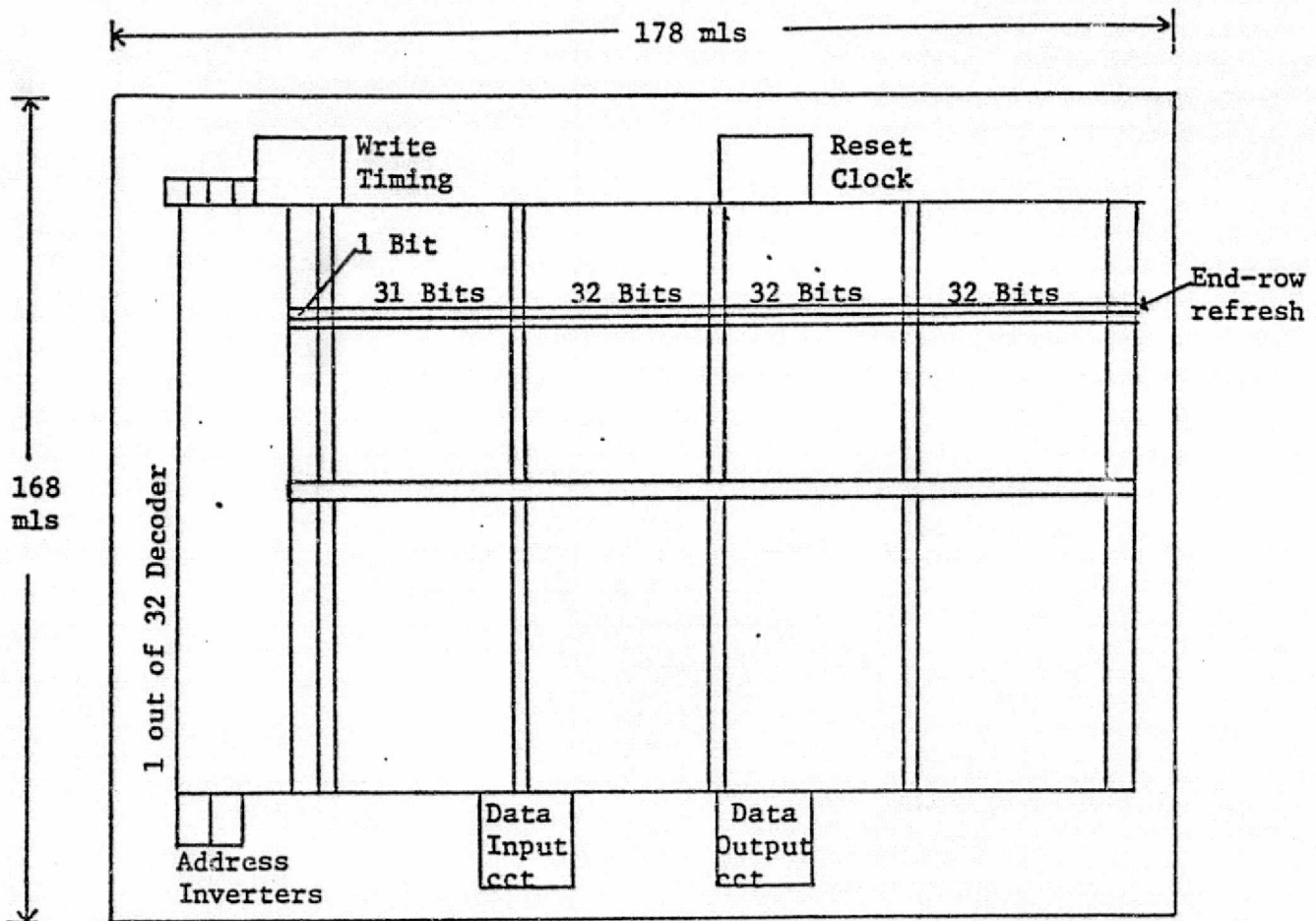


FIGURE 2

CCD Timing Waveforms



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FIGURE 3
Decoded CCD Memory Chip Logic Design

A P P E N D I X B

8192-bit Block Addressable CCD Memory

8192-Bit Block Addressable CCD Memory

STANLEY D. ROSENBAUM AND J. TERRY CAVES

Abstract—Design data and experimental characteristics are given on an 8192-bit n-channel charge-coupled memory device, intended for applications requiring shorter latency than ordinary MOS shift registers or fixed-head disks and at potentially lower cost than either MOS shift registers or random-access memories. This was achieved by dividing the array into 32 memory blocks of 256 bits each, with addressable, random access to any block, permitting average latency of approximately 100 μ s. A two-level overlapping polysilicon gate process was used, with conservative design tolerances. Power dissipation on-chip, plus capacitive drive power during data access at 1 MHz is approximately 250 mW, and less than 5 mW during standby at 20 kHz with data retention.

I. INTRODUCTION

THE 8192-bit (8K) n-channel charge-coupled device (CCD) to be described here was designed for applications requiring shorter latency than ordinary MOS shift registers or fixed-head disks and drums, with low standby power so as to minimize the disadvantage of memory volatility, and at potentially lower cost than either shift registers or MOS random access memories. Conservative tolerances were used, suitable for present-day manufacturing techniques.

A two-level overlapping polysilicon-gate process was used, the same as used for a 4K serial memory CCD which has been described by Ibrahim and Sellars [1]. Whereas that 4K device made use of ratio-type bootstrapped inverters for charge regeneration, the increased packing density required for an 8K chip was made possible by providing charge regeneration circuits of higher sensitivity, which allowed the use of CCD electrodes of smaller area. This was achieved by using ratioless dynamic MOS circuitry, which kept the sensing node capacitances to a minimum, and eliminated dc power drain.

To shorten the latency the array was divided into 32 memory blocks (tracks) of 256 bits each, with addressable, random access to any block through an on-chip decoder. The device was designed to provide data transfer rates up to 2 MHz, but with dc power dissipation minimized, so that at low frequency the power demands of the chip would be small. The lowest possible standby or "idling" power was considered to be an

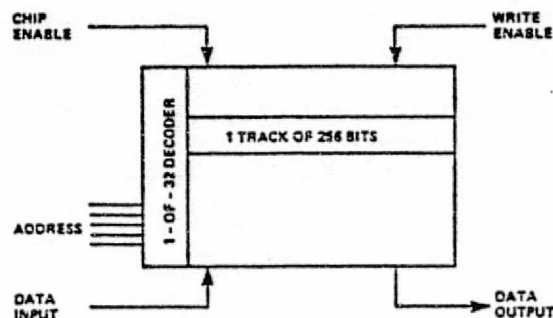


Fig. 1. Overall chip organization: schematic diagram.

important requirement, so that the device could be useful for data retention over long periods. Since this requires a low clock frequency, and to improve the device capability in this respect, charge regenerators were provided at more frequent intervals than would otherwise be needed.

This device is basically, apart from minor modifications, as previously described by the present authors [2].

II. CHIP ORGANIZATION AND CIRCUIT DESIGN

A. Overall Chip Organization

The organization of the chip into 32 memory blocks or "tracks" of 256 bits each, as shown in Fig. 1, provides random access to any track by on-chip decoding of a 5-digit address. A chip enable (CE) input allows the data input and data output terminals of a number of devices to be OR-tied to common buses, including the use of a combined I/O bus if required. A CE LOW state shuts off the power dissipation in the peripheral circuits.

The storage array electrodes are connected so that all tracks are clocked together, which calls for high-power dissipation when fast data access is required, but provides important advantages. One advantage is economy in area, since additional area would be required for providing individual clock connections and steering circuitry. Another advantage is that the data in all tracks are refreshed simultaneously, with no need for periodic addressing of individual tracks. For this reason, the CE input was arranged to affect only the peripheral circuitry involved in data transfer, so that the chip may be

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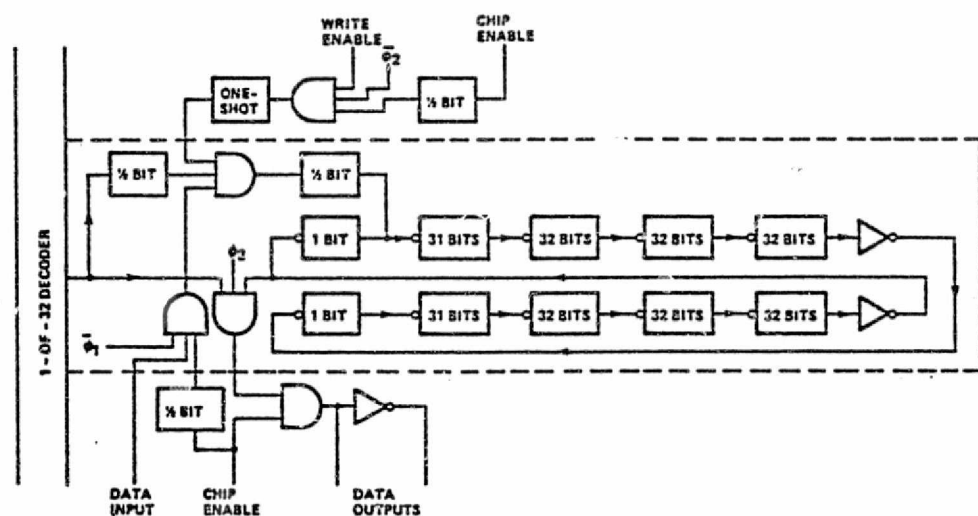


Fig. 2. Logic diagram for one track of 256 bits, and common peripheral circuits.

clocked at a suitable low idling frequency without addressing any track, to maintain data during standby operation. This brings the further advantage that the minimum idling frequency is determined by the average leakage current of all the storage locations on each track, rather than the current at the highest leaking location, which may be an order of magnitude higher in typical as opposed to specially selected chips. A disadvantage of clocking all tracks together is the high capacitance which must be driven, amounting to as much as 700 pF for each of the two principal clock phases, much of this consisting of interelectrode capacitance and active charge-transfer capacitance, between the two phases. This places an economic penalty on high-clock frequencies, regardless of any inherent limitations of the design.

For large block sizes, considerable clock power and also chip area could be saved by using a multiplexed data flow organization such as serial-parallel-serial (SPS), but this would have offered no advantage for a block size as small as 256 bits. A sequential read/modify/write operation was chosen, so that page-swapping and similar data handling techniques were available if required.

In Fig. 2 is shown the organization of a single track, connected to the decoder and to the input and output circuits. Each track is a recirculating serial memory or loop, made up of two parallel rows of 128 bits each. The input and output circuits connect into the serial loop at different points, separated by a 1-bit delay section. This delay is a convenience which provides more time for the read/modify/write operation, and also simplifies the read/write control circuitry, which otherwise would require several additional MOS transistors for each track. In addition to the 1-bit section, each row is broken into a 31-bit and three 32-bit sections, so that all data on the chip are regenerated after 32 clock cycles. This allows for lower idling frequency and therefore lower power, since the fundamental idling power is that which is required to transfer all data through a charge regeneration stage in time to prevent errors caused by leakage currents. For geometrical reasons of layout, both of the 128-bit rows have the same arrange-

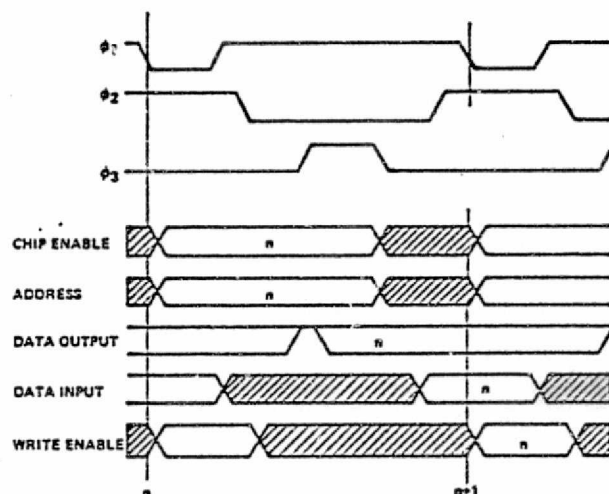


Fig. 3. Timing sequence for clocks, control signals, and data.

ment, including a 1-bit section, which also evens out the number of logic inversions as the data make a complete circuit.

It may be seen in Fig. 2 that sample-and-hold or "1/2-bit" delays are provided in several places outside the recirculating loops. Bearing these in mind, and also by reference to the timing sequence shown in Fig. 3, the read/modify/write operation can be followed. Also shown in Fig. 3 for later reference are the two main clock waveforms, ϕ_1 , ϕ_2 and the auxiliary clock ϕ_3 , all supplied from off-chip, and the reset clock ϕ_R , which is generated on-chip. The existence of CE HIGH at the start of any cycle n causes decoding of the 5-bit track address, and the appearance of an output data bit after a delay which is regulated by the time delay between ϕ_2 OFF and ϕ_3 ON. The state of CE is sampled during ϕ_3 ON [termed *stored chip enable* or (SCE)] by the data input buffer and by the write control circuitry. A high-level SCE will permit writing at the start of the next cycle $n+1$. The input data bit is sampled at that time, and if a decision is made to write, the input data bit replaces the bit which was read out during cycle

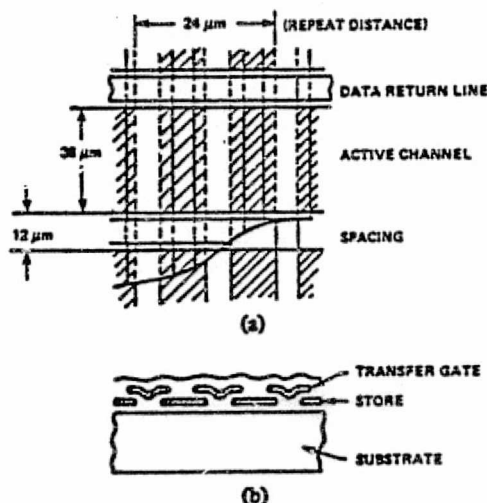


Fig. 4. Basic memory cell: (a) plan view and (b) cross section.

2. To ensure that this always occurs, even when a different track and/or different chip may have been selected for readout during period $n + 1$, the output nodes of the track decoder are also sampled during ϕ_3 , ON, providing stored decode (SD) functions, as represented by the $\frac{1}{2}$ -bit delay SD in Fig. 2.

B. Basic Memory Cell

Plan and cross-sectional illustrations of the basic memory cell are given in Fig. 4. Polysilicon electrodes were preferred for both upper and lower levels, because they provide stable, predictable thresholds, and because they can be photoengraved to close tolerances more easily than aluminum. A further advantage, for the type of device organization chosen, was that aluminum conductors could be situated over the polysilicon electrodes, to transmit data from the output of each end-of-row charge regeneration stage back to the starting side of the array, all transfer of charge being in one direction. This avoided the use of a serpentine organization to transfer charge in opposite directions on adjacent rows, requiring electrode crossovers and resulting extra area and coupling capacitances.

Two-phase overlapping clocks, shown as ϕ_1 and ϕ_2 in Fig. 3 were chosen to operate the basic memory array, the auxiliary clock ϕ_3 not being involved in clocking the basic cell. Although the quantity of charge which can be handled by two-phase clocks is smaller than that possible by four-phase clocks, the two-phase clocks are simpler, and interelectrode coupling effects are minimized, which was an important consideration for the clocking of appreciable capacitance at frequencies up to 2 MHz.

The cell dimensions were chosen with regard to normal manufacturing tolerances in MOS processing, and also with regard to the need for providing sufficient charge for operating the charge regenerators with adequate margins and satisfactory yield.

C. Design Considerations for CCD Arrays

Normal two-phase operation of a CCD using overlapping clocks has been thoroughly discussed by various authors [3], [4]. Input and output conditions suitable for digital opera-

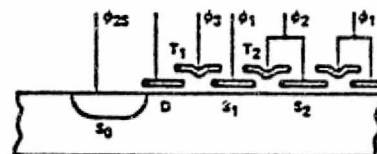


Fig. 5. Charge launching structure in cross section.

tion have been less thoroughly discussed, and it may be in order to summarize here the following considerations which govern the correct manipulation of charge.

1) *Charge Launching*: The quantity of charge which is launched must be properly controlled; too large a quantity causes serious drop in transfer efficiency and resulting errors.

2) *Charge Transfer*: In the present device the charge is regenerated after at most 32 bits (64 transfers) to minimize idling power, so that with proper input charge control the transfer losses are very small, with no need for special measures such as bias charge (fat zero) operation.

3) *Charge Storage*: Low-leakage currents are desired, since these determine the allowable storage time and hence, in conjunction with the number of transfers required to refresh all the data, determine the idling power.

4) *Charge Sensing*: Ratioless dynamic MOS techniques are preferable, since the transistor which evaluates the state of the sensing node can then be of minimum area, minimizing the total node capacitance and providing a satisfactory voltage swing for a given small quantity of charge.

5) *Charge Disposal*: If the sensing node is required to be or could incidentally be driven below MOS threshold voltage by the transfer of charge, this potential may be lower than the surface potential under the last CCD transfer gate. This raises the possibility that some charge may run back into the last store when this is again clocked high, so degrading the noise margin if the last store should in fact be storing a zero level of charge. A good way to prevent this is to reset the sensing node before the last store is again clocked high.

D. Charge Launching and Regeneration Circuits

The structure used for launching and initial transfer is shown in Fig. 5. Charge is made available by the source diode S_0 , which is held at ground potential at time of launching. A launch timing gate T_1 is driven from the auxiliary clock ϕ_3 , and allows launching while the first store S_1 is at high level (ϕ_1 clock) but within the time that the second store S_2 (ϕ_2 clock) and its associated transfer gate T_2 are low. This timing restriction ensures that the amount of charge is controlled only by the first store, with no charge being permitted to enter the second store until launching has been inhibited by turn off of ϕ_3 . Data control gate D is driven from the previous charge regeneration stage, and its state during ϕ_3 ON determines whether charge is launched. No provision was made for a bias charge, and this is not needed since the maximum number of transfers from launching to regeneration is only 64.

Since S_1 receives an equilibrium charge from the grounded source, this quantity of charge would be too great to be handled by two-phase clocking of the main CCD shift register electrodes, if S_1 had equal area to the other electrodes. To con-

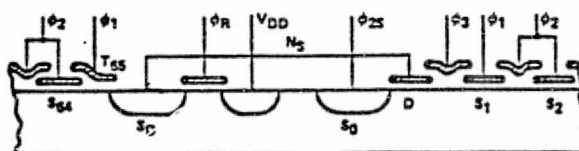


Fig. 6. In-row charge regeneration structure in cross section.

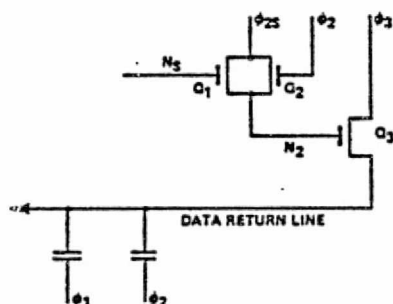


Fig. 7. End-row charge regeneration circuit schematic diagram.

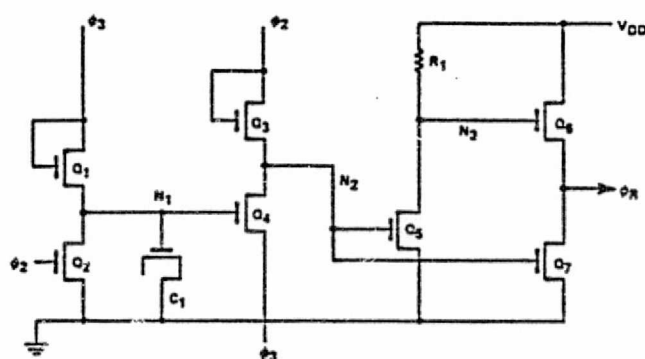


Fig. 8. Reset clock generator: circuit schematic diagram.

trol the charge to a suitable level, S_1 was made about 50 percent smaller in area than the others. As Fig. 5 indicates, the source is not held constant at ground potential but is driven from clock ϕ_{2S} . The purpose of this is explained below, and is not for the purpose of "skimming" the charge in S_1 to the level set by the barrier potential under T_1 , as is sometimes done. Skimming does not occur, because T_1 shuts off with ϕ_3 before the potential on S_0 rises above ground potential.

The structure used for the in-row regeneration of charge is shown in Fig. 6. When ϕ_2 turns off, the last store S_{64} dumps charge into the sensing node N_S composed of sensing diode S_D and data control gate D . Earlier dumping than this is prevented by the barrier potential of the last transfer gate T_{65} . This gate is given by ϕ_1 , although a dc bias would serve equally well. There is no risk that charge may run back from N_S into S_{64} , because N_S is reset to its high potential before S_{64} is again clocked high.

The dumping of charge onto N_S takes the potential of D below threshold prior to ϕ_3 ON, thus inhibiting the launching of charge into the next CCD section. If, however, no charge is dumped into N_S , a full charge is launched into the next CCD section, so that in-row regeneration involves logical inversion.

At the end of each row a more powerful amplifier is required, capable of driving the metallic return line which is loaded by more than 1-pF capacitance to the clock electrodes. Fig. 7 shows a schematic diagram of the three-transistor circuit which performs this function. Its operation is as follows. When ϕ_2 rises, the internal node N_2 is precharged high through Q_2 , because the internal clock ϕ_{2S} has the same timing as ϕ_2 . Q_3 is conducting, and clamps the data return line to the low level of ϕ_3 . When ϕ_2 turns off, Q_2 is shut off and N_2 conditionally discharges to ground (ϕ_{2S} low level) providing Q_1 has not been taken below threshold by the transfer of charge into N_S . The data return line is thus left floating at close to ground potential, and remains unaffected by the rise of ϕ_3 since Q_1 holds the gate of Q_3 at ground potential. If charge has been transferred into N_S , N_2 remains charged, and the rising edge of ϕ_3 boot-

straps node N_2 , allowing the data return line to rise to ϕ_3 clock high level. Because of inversion between nodes N_S and N_2 , and allowing for the inversion between the data control gate and the sensing node of each CCD section, there is an even number of six inversions per row, or twelve inversions around each recirculating loop.

At first sight it might seem that a timing hazard exists, in that N_2 could partially discharge while the charge was still being transferred onto S_D . This is not the case, because charge begins to transfer progressively as ϕ_2 falls, and both theoretical and experimental studies showed that no erroneous discharging could occur if ϕ_{2S} had ϕ_2 amplitude and timing, with fall time no shorter than 10 ns. In fact, the fall of ϕ_{2S} lags slightly behind ϕ_2 , providing an increased safety margin. This, however, is a secondary benefit of using ϕ_{2S} rather than ϕ_2 itself, the main purpose of generating ϕ_{2S} being to provide a pulse which could be connected to all the source diodes also, as shown in Figs. 5 and 6. The advantage of doing this is that when ϕ_{2S} turns off it gives the same capacitive kick to the in-row sensing nodes as to the end-row sensing nodes, ensuring that they work together over the same range of operating conditions. The ϕ_2 clock could have been used directly, but this would have meant that the amount of charge launched would have been sensitive to the ϕ_2 level, whereas ϕ_{2S} is taken on-chip to within a few millivolts of ground during launching.

Attention was paid to the possibility of clock noise on the data return lines, especially because they may be left floating low at launching time. However, this is not a problem, because the significant clock edges occur while the lines are clamped low, except for the falling edge of ϕ_2 which gives an unimportant small downward kick. No noticeable kicks are contributed by ϕ_3 , since this clock has quite negligible capacitance to the data return lines.

As previously mentioned, the sensing nodes are reset high before ϕ_2 HIGH. The reset clock ϕ_R is generated on-chip, using a circuit shown schematically in Fig. 8. Its operation is

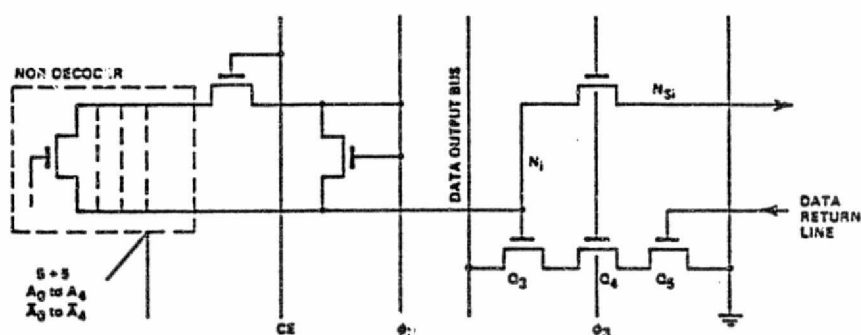


Fig. 9. Schematic diagram of address decoder, data readout, and stored decode circuit for one track.

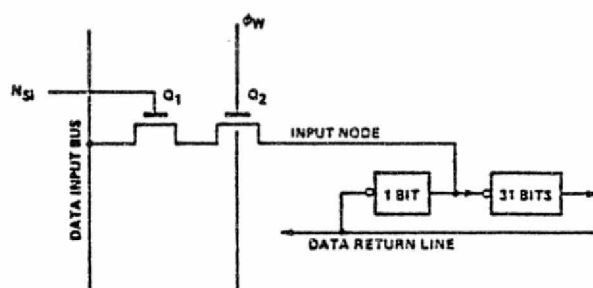


Fig. 10. Schematic diagram of write control circuit for one track.

as follows. Between the fall of ϕ_2 and the rise of ϕ_3 , nodes N_1 and N_3 are low, node N_2 is high, and the output ϕ_R is low. N_1 is charged high by the rise of ϕ_3 , and remains high until the rise of ϕ_2 . N_2 remains high during ϕ_3 HIGH, and falls with ϕ_3 , causing N_3 to rise, bringing ϕ_R high with it. Output transistors Q_6 and Q_7 provide high conductance paths which conduct at different times.

E. Address Decoding and Data Readout

The decoder is a NOR gate design, as shown in Fig. 9 for a representative memory track. All decoder output nodes such as N_i in Fig. 9 are precharged high during ϕ_2 HIGH, and selection of the addressed node follows the fall of ϕ_2 , all unselected nodes discharging to ϕ_2 LOW. To minimize power dissipation the address inverters have low aspect ratios, and drive the decoder through capacitor-pumped boosters. The data output bus is precharged high during ϕ_2 ON, and conditionally discharged during ϕ_3 ON by the readout AND gate Q_3 , Q_4 , and Q_5 of the addressed track, according to the state of the data return line. The state of the data output bus during ϕ_3 ON is communicated to the data output terminal through an amplifier which is provided with an optional latch. When no data access is required (CE LOW) all significant power drain is eliminated from the decoder and readout circuits.

F. Write Control Circuitry

Referring to Fig. 10, the data input bus is precharged during reset time by clock ϕ_R , and conditionally discharged during ϕ_1 LOW if the data input terminal is high, and if stored chip enable (SCE) is high, i.e., if the need for data transfer was

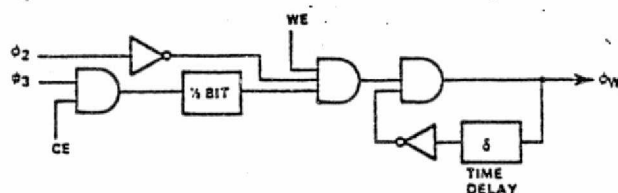


Fig. 11. Logic diagram for write-strobe clock generator.

signaled previously by holding CE high during ϕ_3 HIGH. The states on the decoder output nodes N_i are sampled during ϕ_3 HIGH to provide the stored decode signals N_{Si} . One of the nodes N_{Si} will store a high level, to identify one track for writing, and to ensure that this is the same track from which readout was obtained during ϕ_3 HIGH. The final instruction to write is made by ensuring that write enable (WE) is high at the time that ϕ_2 falls. This instruction will only take effect if SCE is high; if it is, an internal write-strobe clock ϕ_W is activated, and the state of the input data bus is communicated to the input node of the selected track via one of the AND gates such as is shown in Fig. 10, comprising transistors Q_1 and Q_2 .

The write-strobe clock is generated by a one-shot timing circuit, based on a form of digital negative feedback through a delay circuit, as shown schematically in Fig. 11. After ϕ_2 falls, ϕ_W rises rapidly, to be shut off again as soon as the output of the delay network has risen significantly above threshold.

The input node of each track is also the sensing node of the first 1-bit section. If no writing is conducted, the state of the sensing node is defined only by the transfer of charge from the 1-bit. However, when writing into the track, the state of the sensing node is controlled by the state of the data input bus.

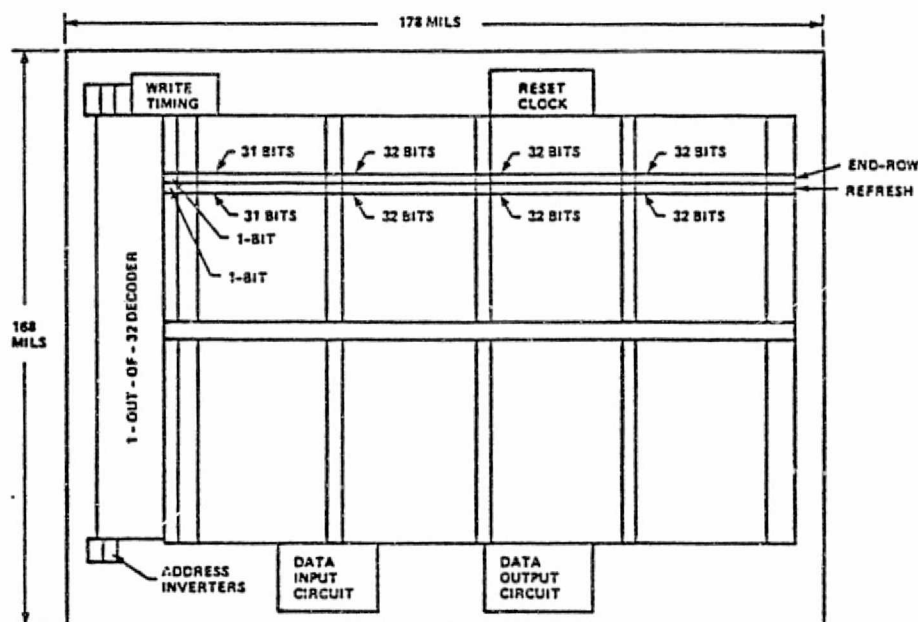


Fig. 12. Chip layout diagram, showing location of principal features.

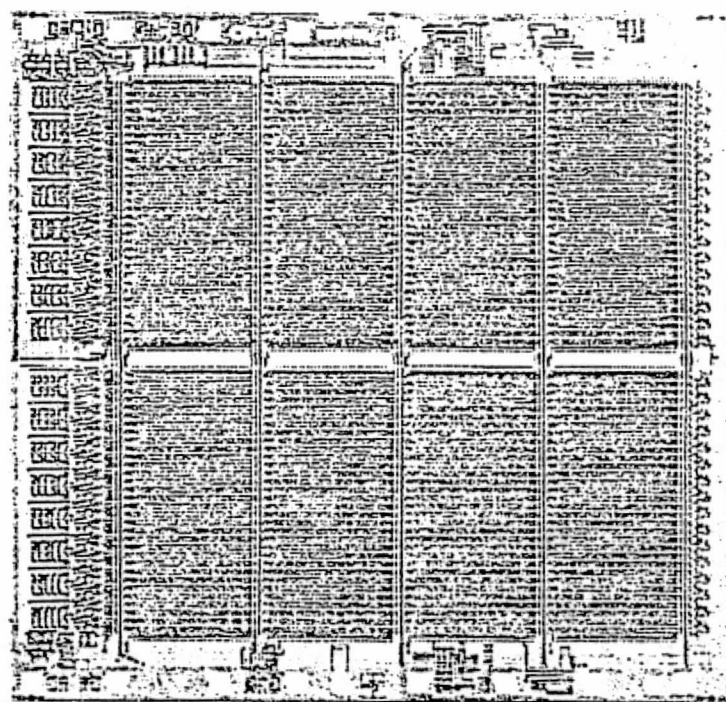


Fig. 13. Photograph of 8K CCD memory chip.

G. Chip Layout

Location of the principal circuit features is shown in Fig. 12, and a photograph of the chip is shown in Fig. 13. The overall chip dimensions of $178 \times 168 \text{ mil}^2$ result in an average area of $3.6 \text{ mil}^2/\text{bit}$. Of this total, the active memory area accounts for $1.4 \text{ mil}^2/\text{bit}$, space between rows accounts for $0.45 \text{ mil}^2/\text{bit}$, charge regenerators account for $0.27 \text{ mil}^2/\text{bit}$, and the decoder accounts for $0.24 \text{ mil}^2/\text{bit}$. The peripheral region of the chip

contains peripheral circuits, interconnections, bonding pads, and unused area, and together these account for $1.2 \text{ mil}^2/\text{bit}$ of the total average area. As is usual in low-threshold n-channel MOS circuits, the 8K CCD was designed to operate with a negative dc bias on the substrate relative to MOS ground (V_{SS}), with clock low levels close to V_{SS} . This provided the usual beneficial effects on the MOS circuitry, i.e., a convenient working threshold of about 1.5 V under normal conditions of

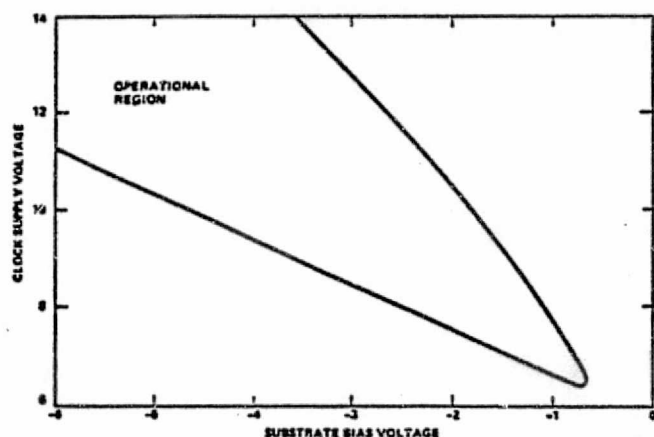


Fig. 14. Operational range of power supply voltages at room temperature under the data integrity test, at clock rates of 10 kHz, 100 kHz, and 1 MHz. For the particular device illustrated the range was the same at all three clock rates.

operation, and wider depletion layer thicknesses, resulting in reduced nodal capacitances and consequently higher speed. However, the effect of substrate bias on the threshold of the upper level polysilicon CCD transfer gates is greater than on the lower level storage electrodes and MOS gates, as a result of the thicker dielectric and consequently greater bulk effect. This was taken into account in choosing the dielectric thickness, so that the proper threshold was obtained under working conditions.

III. TEST RESULTS

Experimental characterization has been conducted over a range of conditions, using clock amplitudes from +6 V to +15 V relative to V_{SS} , clock rates from 100 Hz to greater than 2 MHz, and temperatures from -55°C to $+125^{\circ}\text{C}$. For most of the tests, correct operation was proven at each operating point, using a "data integrity test" based on the techniques which have been devised for random-access memories. For this test, a background of zeros or ones was first written into all 8192 storage elements. Then, for each track in turn, a single complementary bit (one or zero) was written into a track, and the complete contents of the memory were read out and checked for integrity. This complementary bit was then removed, before continuing with the next track. The background was then reversed to the complementary state, and the complete test repeated. An example is shown in Fig. 14 of the operating range of clock supply voltage versus substrate bias observed on a good device under the data integrity test, at clock rates of 10 kHz, 100 kHz, and 1 MHz. Another example is shown in Fig. 15, for a fixed clock rate of 1 MHz and temperatures from -55°C to $+125^{\circ}\text{C}$. At low clock rates this test is time consuming, e.g., almost 1 min at 10 kHz for each operating condition examined, and most characterization at frequencies below 10 kHz was done using less stringent tests. However, good devices have been shown to pass the data integrity test at frequencies down to 400 Hz. In all the tests reported above, the different clock rates were obtained by varying a single parameter, viz., the delay time between fall of ϕ_3 and rise of ϕ_2 , corresponding to one recom-

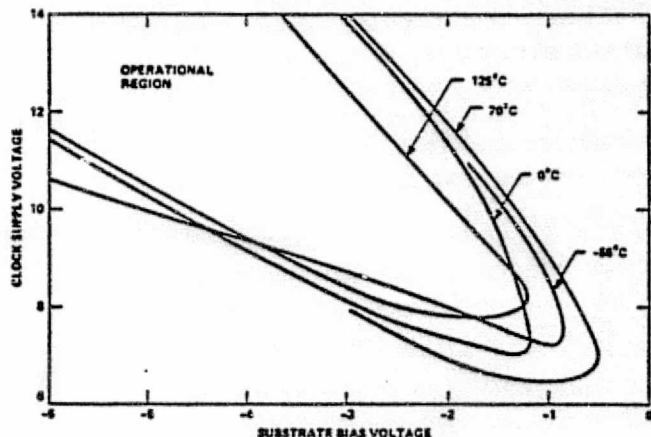


Fig. 15. Operational range of power supply voltages under data integrity test at a clock rate of 1 MHz, for various temperatures from -55°C to $+125^{\circ}\text{C}$.

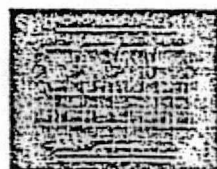


Fig. 16. Waveforms of applied clocks and data output, at a clock rate of 2 MHz. From top: ϕ_1 , ϕ_2 , ϕ_3 and data output. Horizontal scale 200 ns/div, vertical scale 10 V/div.

mended manner of changing between data access mode and idling mode. Correct operation has also been demonstrated at clock rates up to 3 MHz, although a practical limit of 1.5 MHz is regarded as realistic, allowing for clock timing skews and for the economic desirability of driving a number of CCD chips from a set of clock drivers. As an example of higher speed operation, Fig. 16 is a photograph of the applied clock waveforms and output data, at a clock rate of 2 MHz. Under the conditions of the photograph, the operating range of clock supply voltage for this device was found to cover +8.2 V to +12.4 V, at -2 V substrate bias.

The actual operating window of a device which is free from processing defects is limited by principally three mechanisms. One mechanism is that at substrate bias close to zero the transfer of a full charge onto a sensing node may not be sufficient to bring its potential below threshold of gate D of Fig. 6, or transistor Q_1 of Fig. 7. A second mechanism is that at high (negative) substrate bias the upper polysilicon threshold may not be reached at normal ϕ_3 clock amplitude, (see Fig. 6), thus preventing the launching of charge. Figs. 14 and 15 show the effects of these two mechanisms on all the sensing nodes and launching gates on the particular devices referred to in these figures. A third limiting mechanism may occur at a combination of high clock amplitude and high (negative) substrate bias, when the resulting high surface potential relative to substrate at the empty storage locations may cause leakage currents, and consequent errors. In good devices at room temperature this effect may not be noticed, except at very low clock frequencies.

It was of interest to examine the device for possible pattern

sensitivity, especially its behavior under the extreme conditions of being either completely empty or completely full of charge at a given instant. Because of the logic inversions at each in row charge regenerator, these conditions are not brought about by the memory integrity test as defined above, but a close approximation to them was created as follows. The "empty" condition was created by gating clock ϕ_3 off for more than 32 cycles, so that all registers were completely emptied of charge (since the launching of new charges was inhibited). The "empty" state corresponds to a stored pattern consisting of alternate blocks of "1's" and "0's," the same pattern existing on every track. During recirculation the logical inversions cause the total amount of charge transferred per cycle to increase from zero to a maximum, and back to zero again, repeating every 64 cycles. The operating range for storage of such patterns was found to be almost identical to the range for the data integrity test, and the same was true for a variety of 32-bit and 256-bit test words which were also tried.

The essential power required to drive the device consists mainly of capacitive drive power, which is about 200 mW using +12-V clocks at 1-MHz frequency. This power is dissipated off-chip, provided the ϕ_1 and ϕ_2 clock transition times are slow compared to the internal time constant of the long polysilicon electrodes, which is estimated as not exceeding 7 ns. This condition is approximately satisfied, since the transition times need be no shorter than 30 ns to achieve the maximum frequencies, and transition times up to 100 ns may be used.

The total on-chip dissipation is about 50 mW, using +12-V clocks at 1 MHz. About 25 mW of this consists of dc current drain in the peripheral data access circuits, and most of the remainder is dissipated by the resistor R_1 in the reset clock ϕ_R . Because the current drain by R_1 is shut off when ϕ_R is ON, the chip dissipation when no data access is required can be minimized by idling at a low frequency, using a timing cycle which stretches the duration of ϕ_R ON. For example, at 20 kHz the duty cycle of ϕ_R ON can easily exceed 98 percent, and the power consumption then falls to less than 5 mW at +12-V clocks, most of this being capacitive drive power.

IV. CONCLUSIONS

The basic objective has been achieved of demonstrating that a CCD technology could be combined with MOS logic and support circuitry to provide data storage with short latency and low standby power. The favorable characteristics of the device can be attributed to the choice of a fabrication process using double-layer polysilicon plus single-layer aluminum, combined with the efficient use of MOS dynamic circuitry of low power dissipation. It remains to be seen whether the clocking scheme chosen, by which all memory blocks are clocked together, and hence no specific refresh cycle is required, will be preferred by systems designers over the alternative of clocking only the block (or blocks) being accessed.

ACKNOWLEDGMENT

The authors wish to express their thanks to D. R. Colton and K. L. Mayer for proposing the project and for their technical contributions to it, to J. J. White as principal architect of the double-layer polysilicon gate process, to A. A. Ibrahim and L. Sellars for consultations, and to K. H. Siemers, R. Wallace, B. Millar, and D. E. Brown for the major share of the testing and characterization.

REFERENCES

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- [3] W. F. Kosonocky and J. E. Carnes, "Two-phase charge-coupled devices with overlapping polysilicon and aluminum gates," *RCA Rev.*, vol. 34, p. 164, 1973.
- [4] A. M. Mohsen, T. C. McGill, and C. A. Mead, "Charge transfer in overlapping gate charge-coupled devices," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 191-207, June 1973.



Stanley D. Rosenbaum was born in London, England. He received a degree in physics from London University, London, England, in 1952 and graduated from the University of Ottawa, Ottawa, Ont., Canada, in 1972.

He has experience in the design of electronic test equipment and has conducted research on semiconducting elements, compounds and alloys. Since 1958 he has been actively involved in the development of many kinds of semiconductor devices, including bipolar transistors and diodes, microwave varactor diodes, JFET's, MOS devices and digital bipolar integrated circuits. Since 1972 he has worked on the development of charge-coupled devices (CCD's) and is presently Manager of a design team engaged in the development of CCD memories and signal processing devices.



J. Terry Caves was born in Ottawa, Ont., Canada in 1947. He graduated from Algonquin School of Applied Arts and Technology, Ottawa, Ont., Canada.

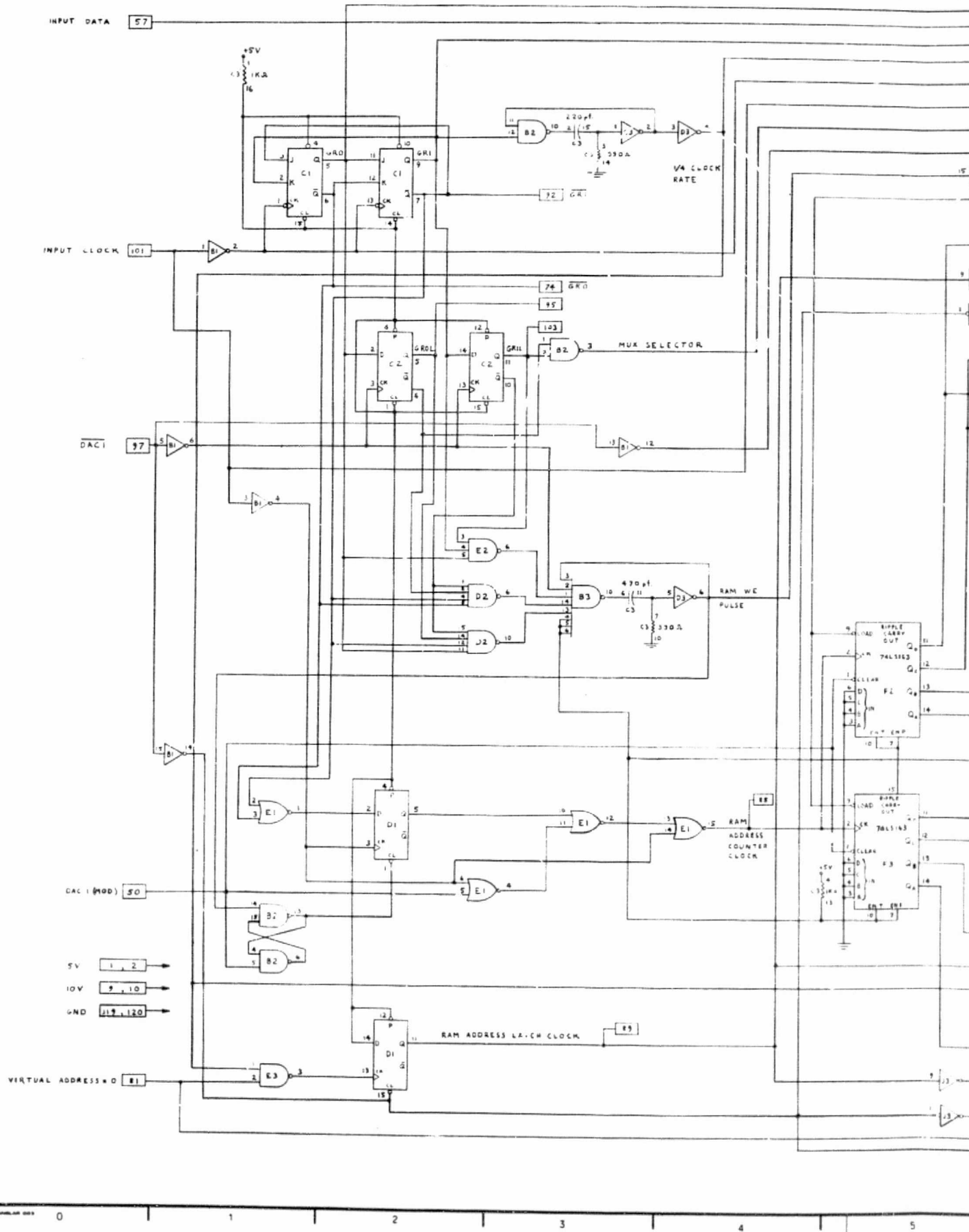
He joined Bell-Northern Research Ottawa, Ont., Canada, in 1969 where he was involved in the development of a p-n-p-n air isolated integrated crosspoint switch, which was intended for wide-band telephone system applications and aroused widespread interest. Since 1971 he has been involved in Bell-Northern's CCD development program, concentrating mainly on digital applications and MOS support circuitry.

A P P E N D I X G

Memory System Schematics

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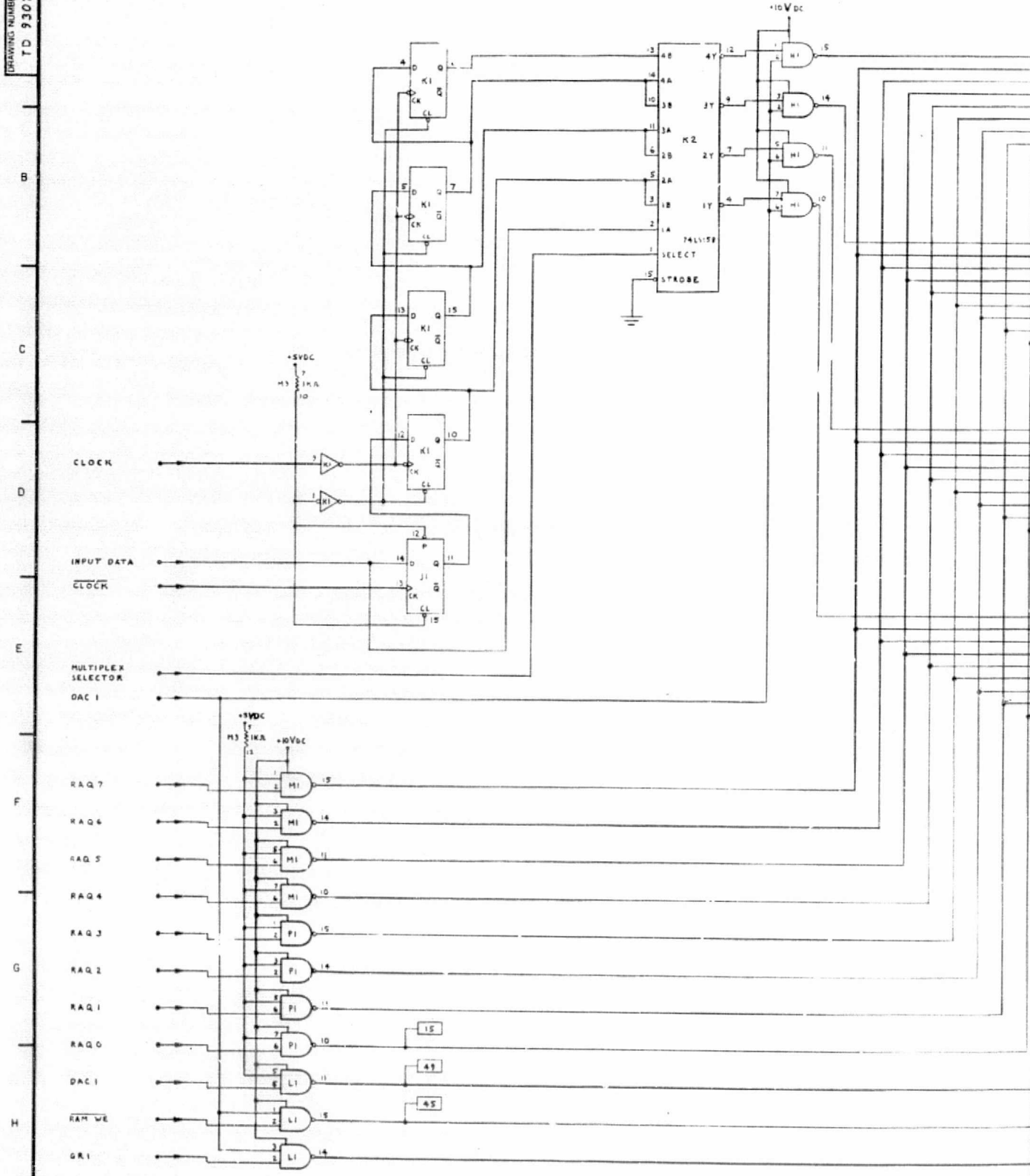


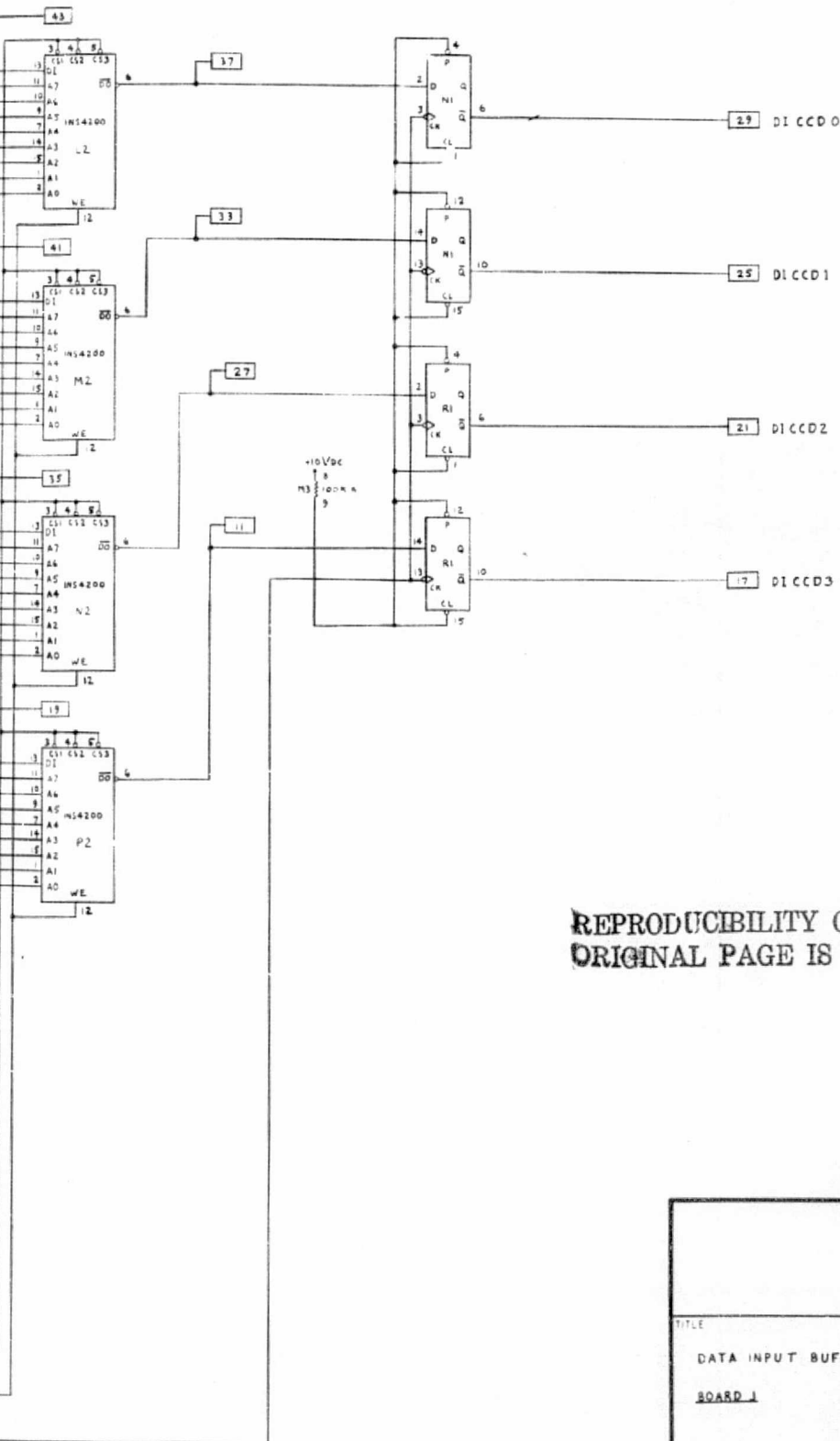


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ISSUE	AUTHORIZATION
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FOR IC LAYOUT,
SEE SHEET 1.

TITLE
DATA INPUT BUFFER

BOARD 1

DESIGN AUTHORITY
Bell - Northern Research

RATING

DRAWING NUMBER

TD 9302

SIZE	SHEETS	SHEET
6S	16	C-2

D100

FOLDOUT FRAME

DRAWING NUMBER
TD 3302
SHEET
3

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H

1/4 CLOCK RATE 31
DAC 1 27
WRITE 27
DATA AVAILABLE 27
MEMORY OVERFLOW 102
DATA O/P AVAIL 46

RESET 75

CE0 57

CE1 58

CE2 53

CE3 51

BANK 0 IN USE 49

BANK 1 IN USE 47

BANK 2 IN USE 48

BANK 3 IN USE 43

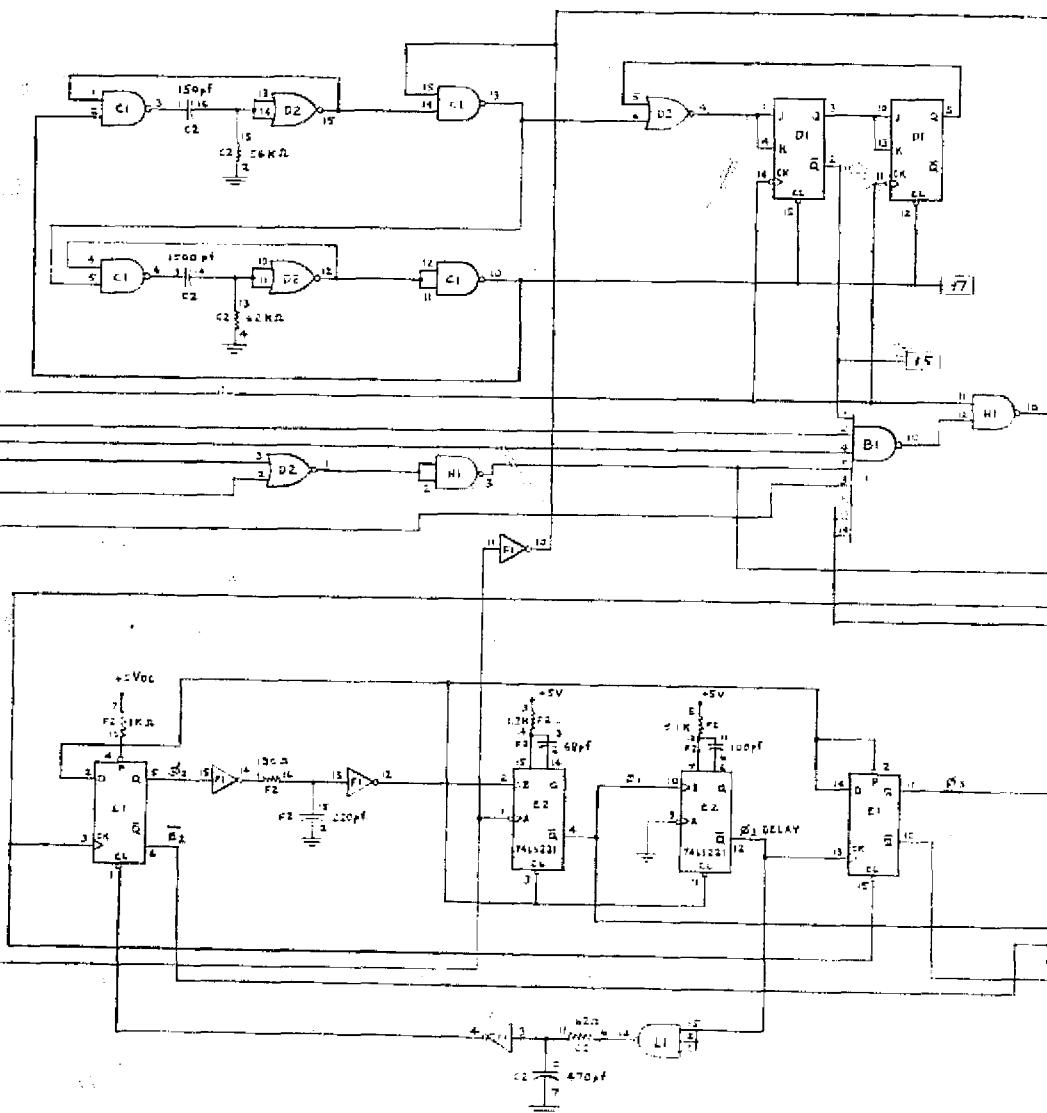
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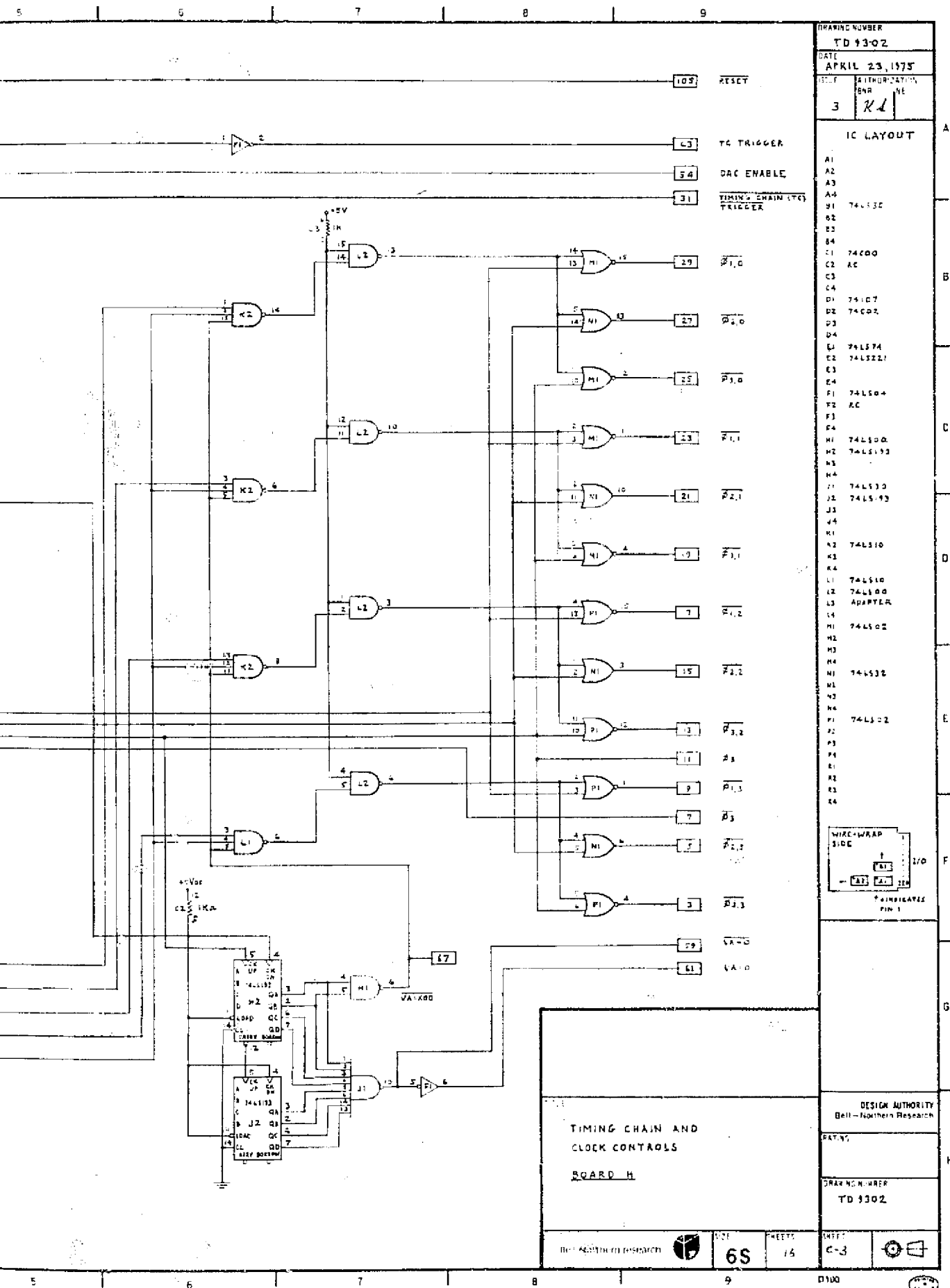
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CE2 39

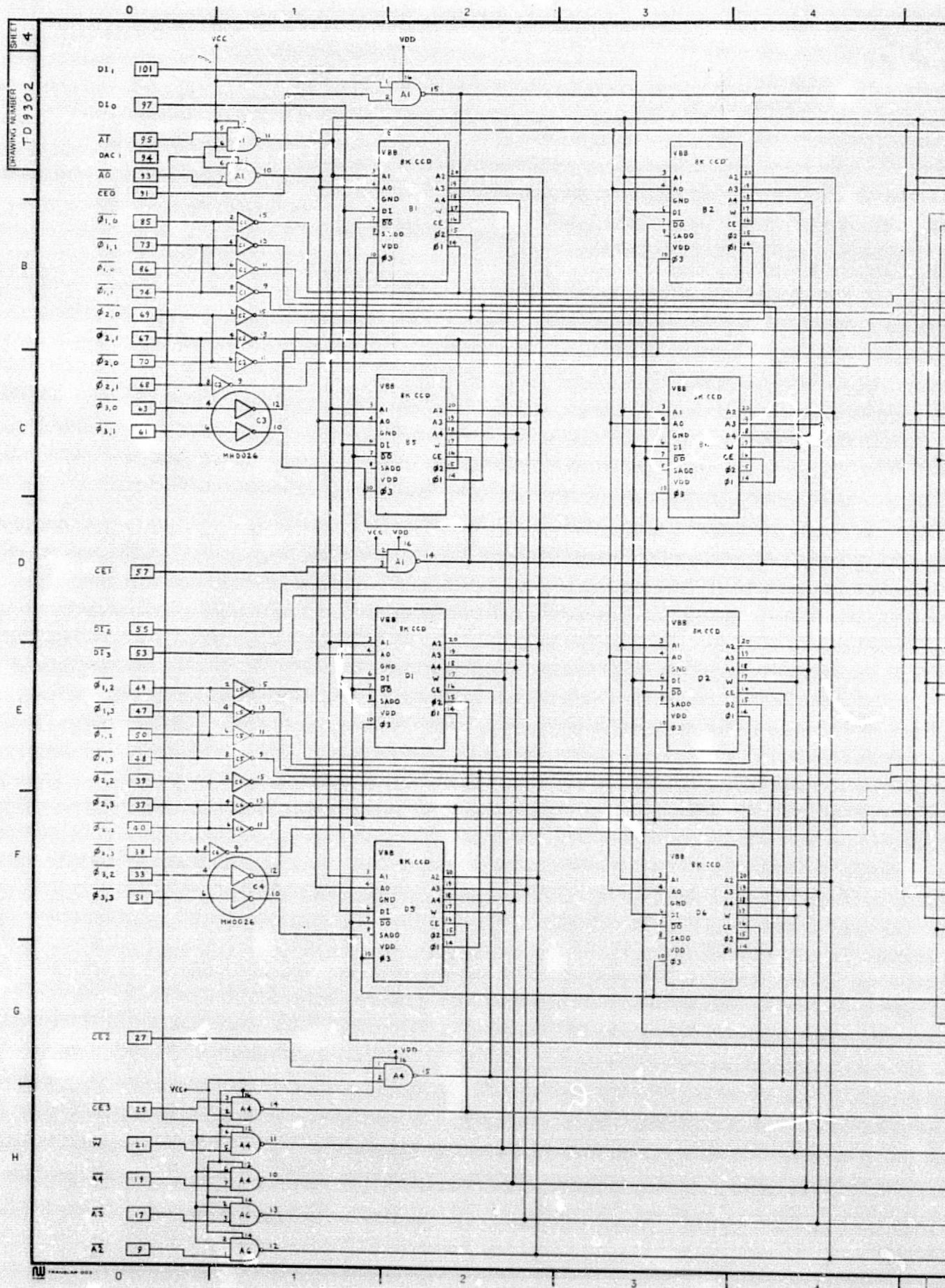
CE3 35

TRANSFER REQUEST 32

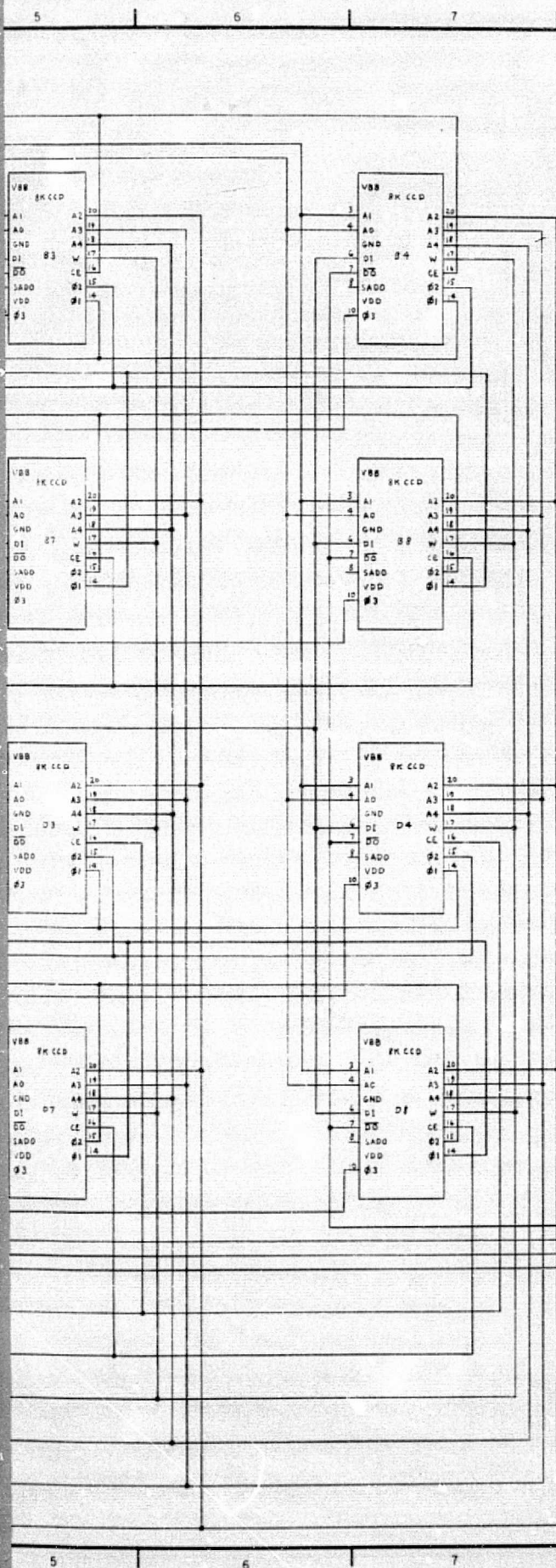




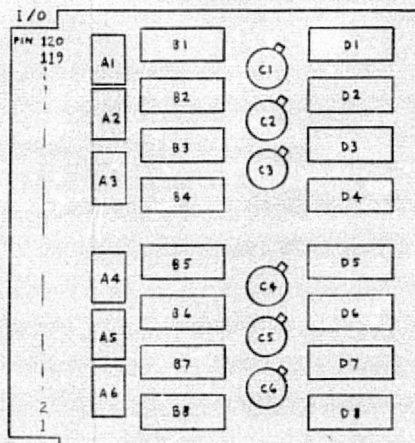
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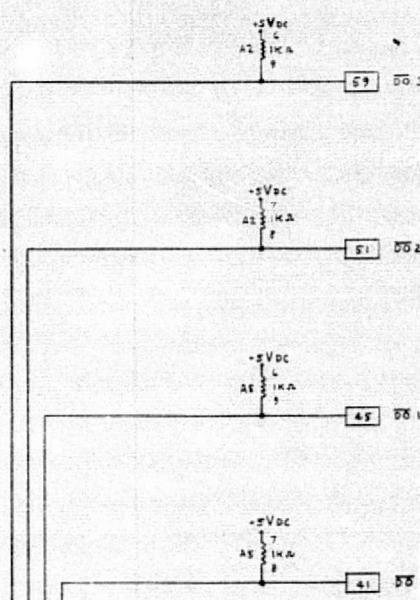
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BOARD LAYOUT (WIRE-WRAPSIDE)



VDD ON PINS 43, 44
VBB ON PINS 79, 80



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TD 9302

DATE
APRIL 24, 1975

ISSUE
3

AUTHORIZATION
BMR

IS LAYOUT

A1 75361A
A2 R
A3
A4 75361A
A5 R
A6 75361A
B1 8K CCD
B2 8K CCD
B3 8K CCD
B4 8K CCD
B5 8K CCD
B6 8K CCD
B7 8K CCD
B8 8K CCD
C1 MH0026
C2 MH0026
C3 MH0026
C4 MH0026
C5 MH0026
C6 MH0026
D1 8K CCD
D2 8K CCD
D3 8K CCD
D4 8K CCD
D5 8K CCD
D6 8K CCD
D7 8K CCD
D8 8K CCD

NOTES:
1. INT. CAPACITORS
ARE USED FOR
DECOUPLING
VDD TO GROUND
AND VBB TO GROUND
RESIDE EACH 8K
CCD AND MH0026.
2. PIN 8 OF EACH
CCD IS TIED
TO VDD.

TITLE
CCD MEMORY BOARD
BOARD F

DESIGN AUTHORITY
Bell-Northern Research

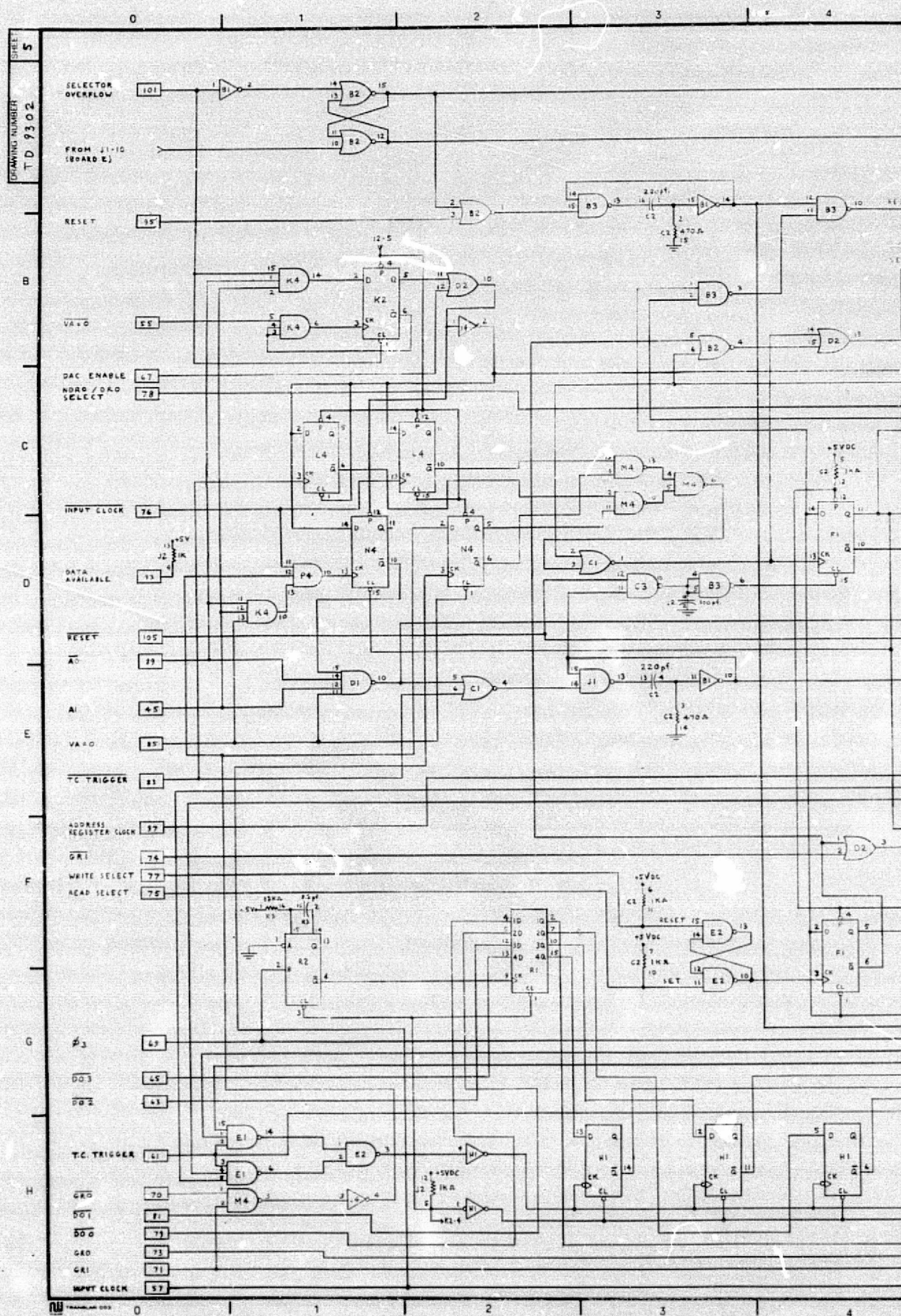
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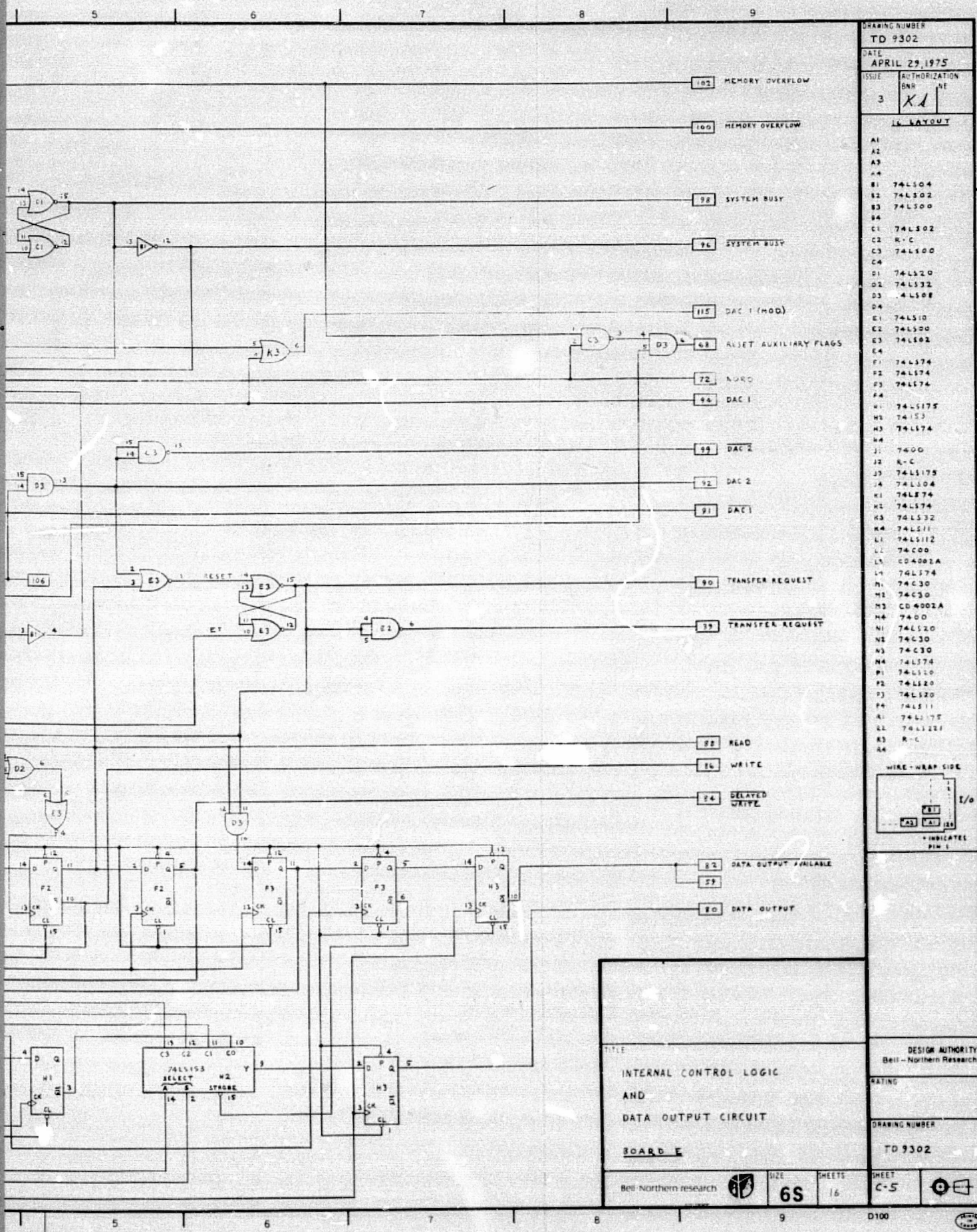
Bell-Northern
6S
SHEETS
16
SHEET
C-4

D100

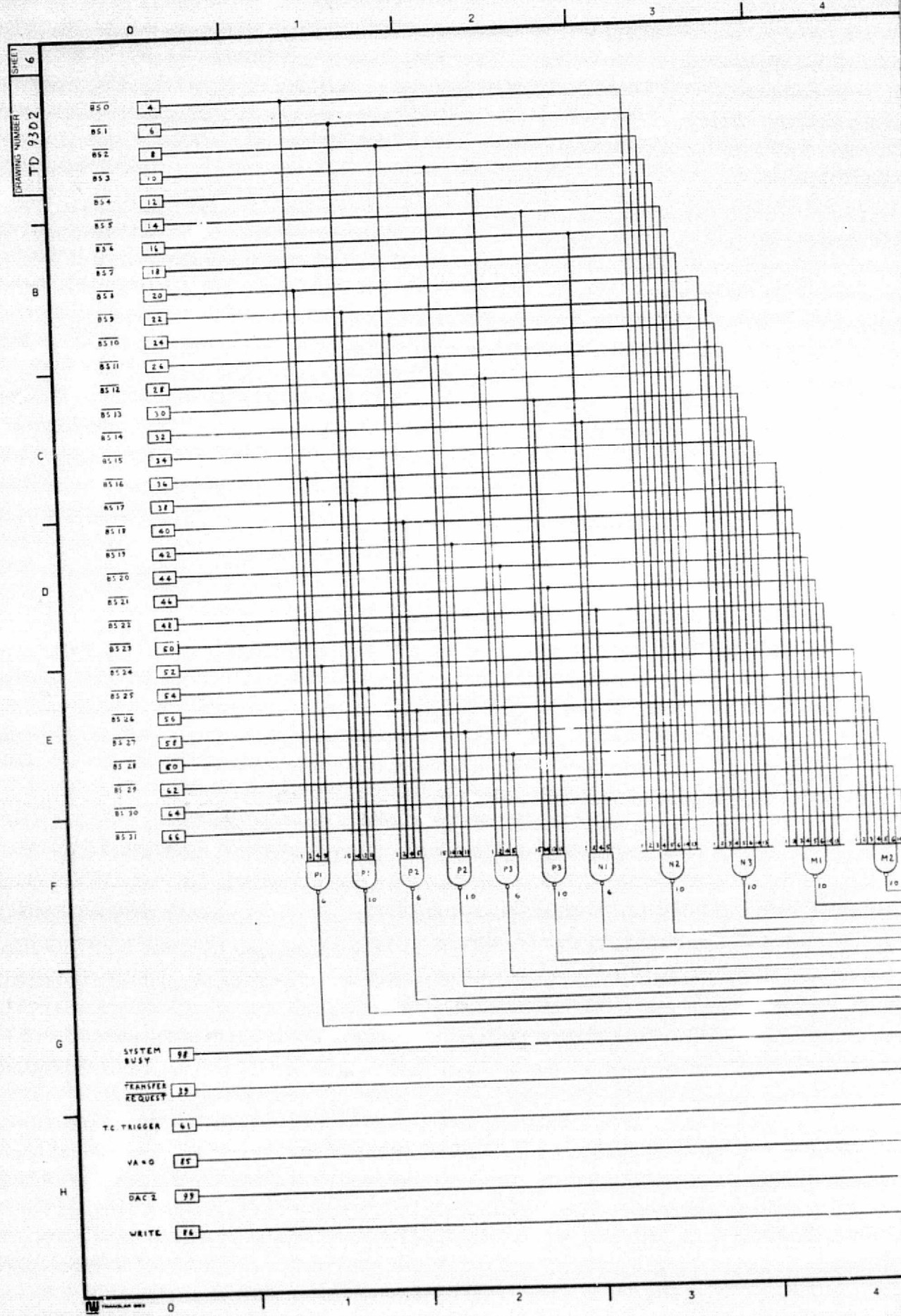
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B3	74LS00	
B4		
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C4		
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D3	74LS08	
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H7	74LS11	
H8	74LS112	
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H11	74LS74	
H12	74C30	
H13	CD4002A	
H14	7400	
H15	74LS20	
H16	74C30	
H17	74C30	
H18	74LS74	
H19	74LS10	
H20	74LS20	
H21	74LS20	
H22	74LS11	
H23	74LS175	
H24	74LS22	
H25	R-C	
H26		
WIRE-WRAP SIDE		
I/O		
* INDICATE PIN 1		
TITLE		INTERNAL CONTROL LOGIC AND DATA OUTPUT CIRCUIT
BOARD E		
DESIGN AUTHORITY		Bell-Northern Research
RATING		
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Bell-Northern research		
SIZE		6S
SHEETS		16
SHEET		C-5
D100		



5

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9

31 NEXT CE0
29 NEXT CE1
15 NEXT CE2
3 NEXT CE3
5 CE3
7 CE2
9 CE1
11 CE0
15 CE3
21 CE0
19 CE1
17 CE2

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DATE
APRIL 25, 1975
ISSUE
3
AUTHORIZATION
BNR
AE
K.L.
FOR IC LAYOUT,
SEE SHEET 5

51 NEXT A2
41 NEXT A3
37 A2
37 NEXT A4
35 A3
13 A2
25 A3
17 A4
33 A4

43 A0
45 A1
47 A2
49 A3

17 ADDRESS REGISTER
CLOCK
53 FLAG CLOCK

TITLE
ADDRESS AND CHIP ENABLE
DECODER

BOARD E

DESIGN AUTHORITY
Bell - Northern Research

RATING

DRAWING NUMBER
TD 9302

BNR Northern research



SIZE
6S

SHEETS
16

SHEET
C-6

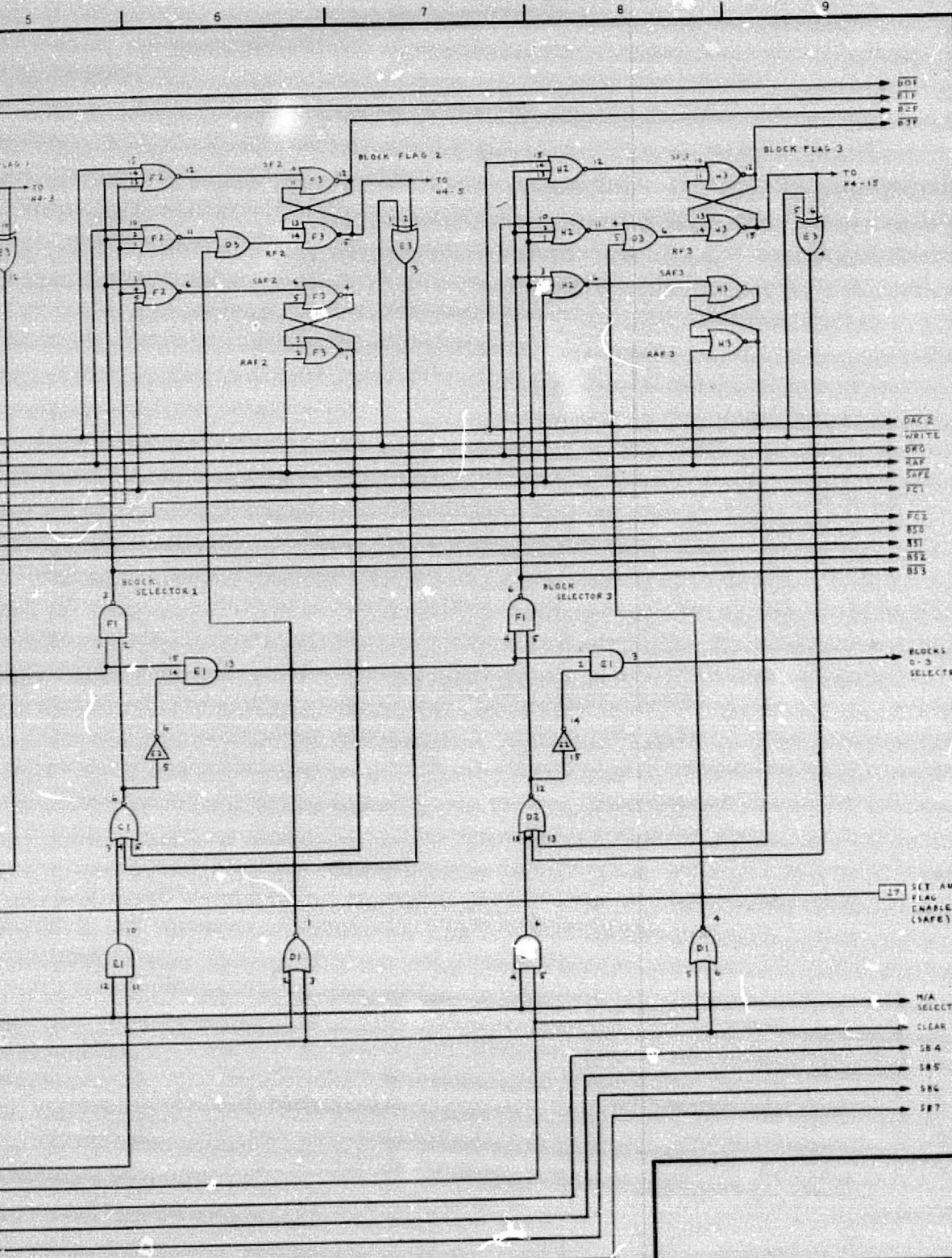


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		B3 74LS02
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		C4
		D1 74C02
		D2 4025
		D3 74LS32
		D4
		E1 74C08
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		F7 74LS02
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		F97 74C04
		F98 74C02
		F99 74LS04
		F100 74LS32

TITLE
BLOCK SELECTOR AND
BLOCK FLAGS FOR
BLOCKS 0 TO 3

BOARD D

bell Northern research

DESIGN AUTHORITY
Bell Northern Research

RATING

DRAWING NUMBER
TD 9302

SIZE 6S

SHEETS 16

SHEET C-7

D100

McGraw-Hill

SHEET 9
DRAWING NUMBER TD 9302

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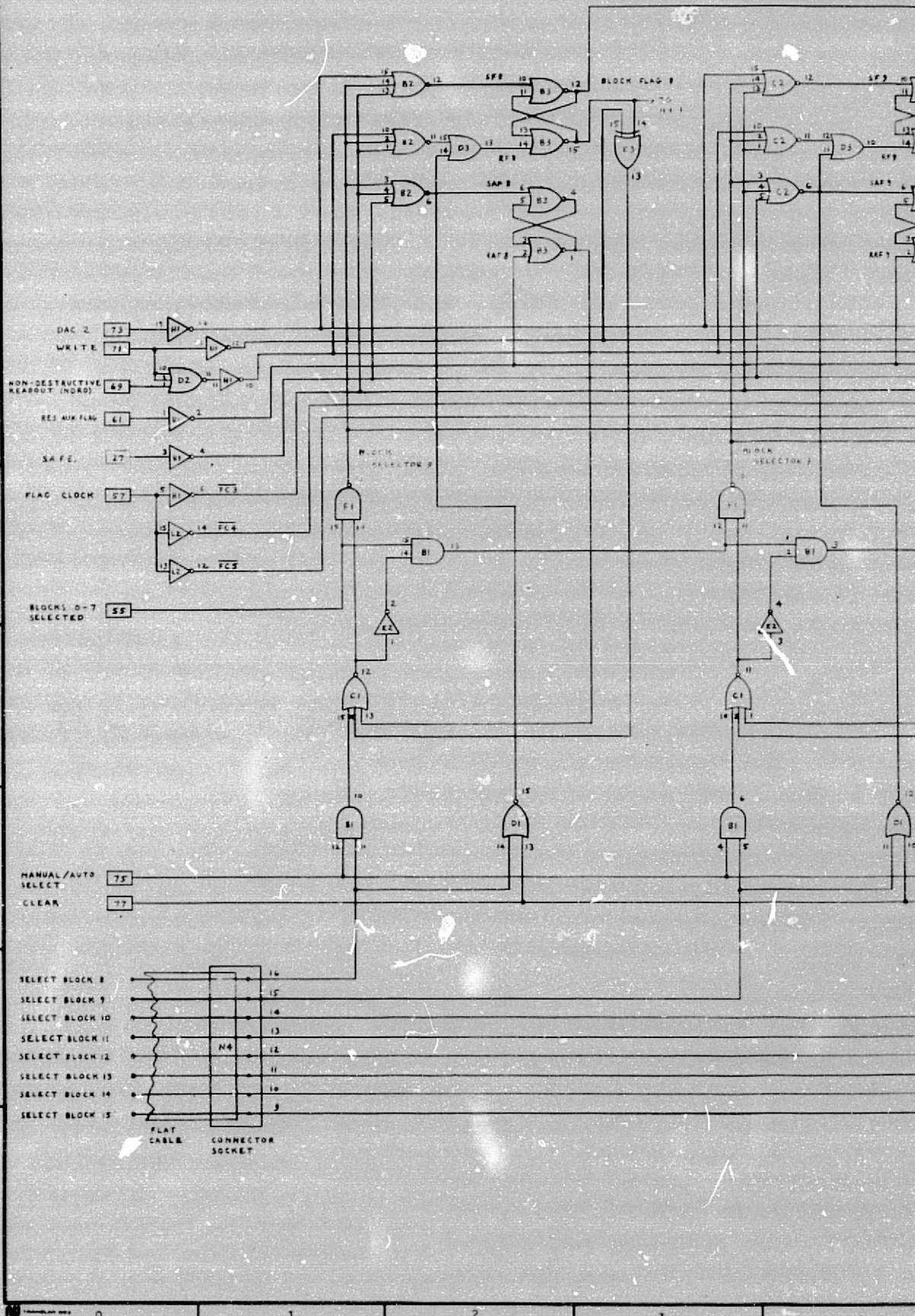
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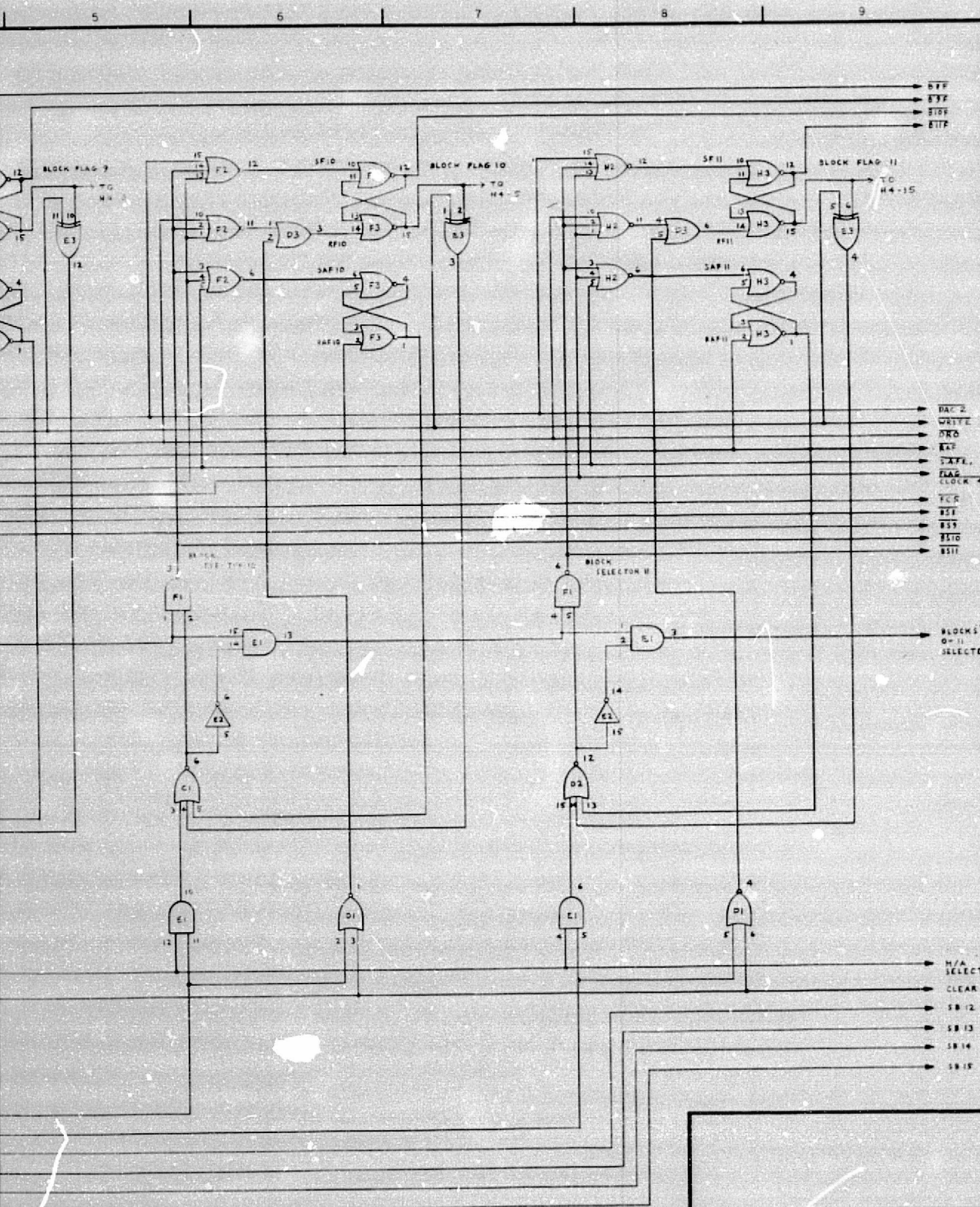
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DATE APRIL 29, 1975	
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FOR 1:1 LAYOUT,
SEE SHEET 7

TITLE
BLOCK SELECTOR AND
BLOCK FLAGS FOR
BLOCKS 8-11

BOARD C

DESIGN AUTHORITY
Bell-Northern Research

RATING

DRAWING NUMBER
TD 9302

Bell-Northern research	6S	16	C-9
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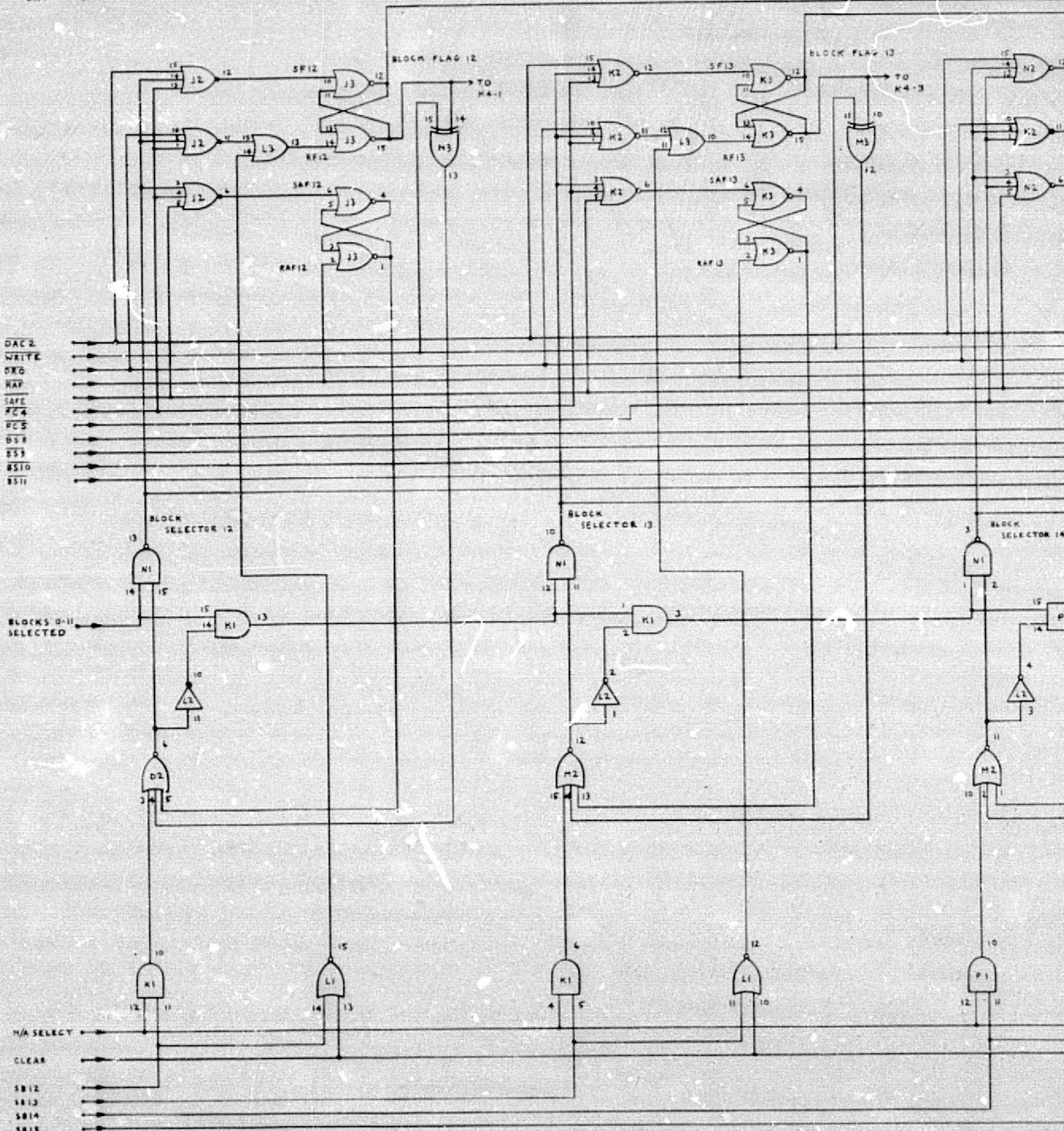
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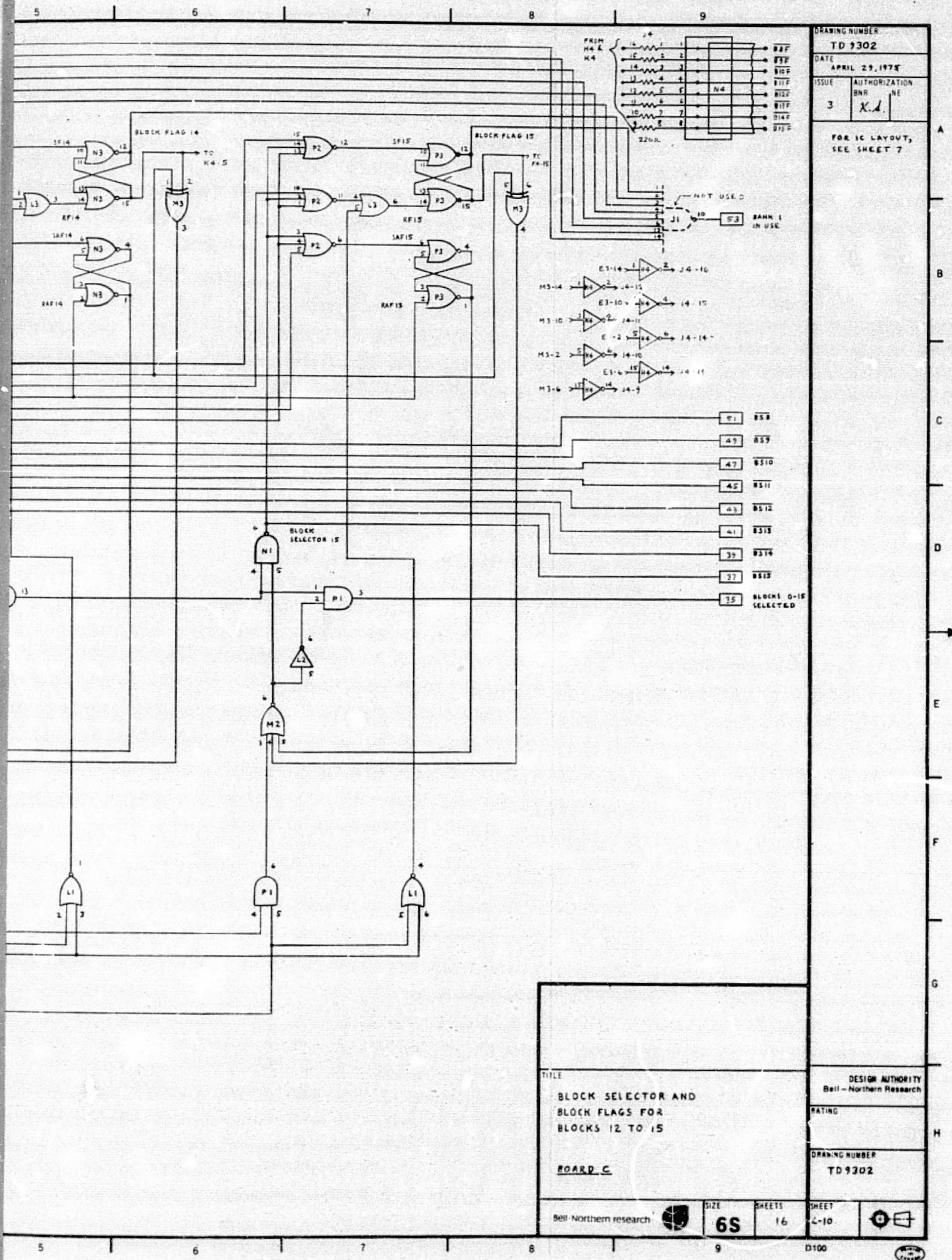
MTT
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BIOF
BTF

DAC2
WRITE
ORG
RAP
SAFE
PC4
PC5
DSR
SS1
SS10
SS11

BLOCKS 0-11
SELECTED

M/A SELECT
CLEAR
SB12
SB13
SB14
SB15

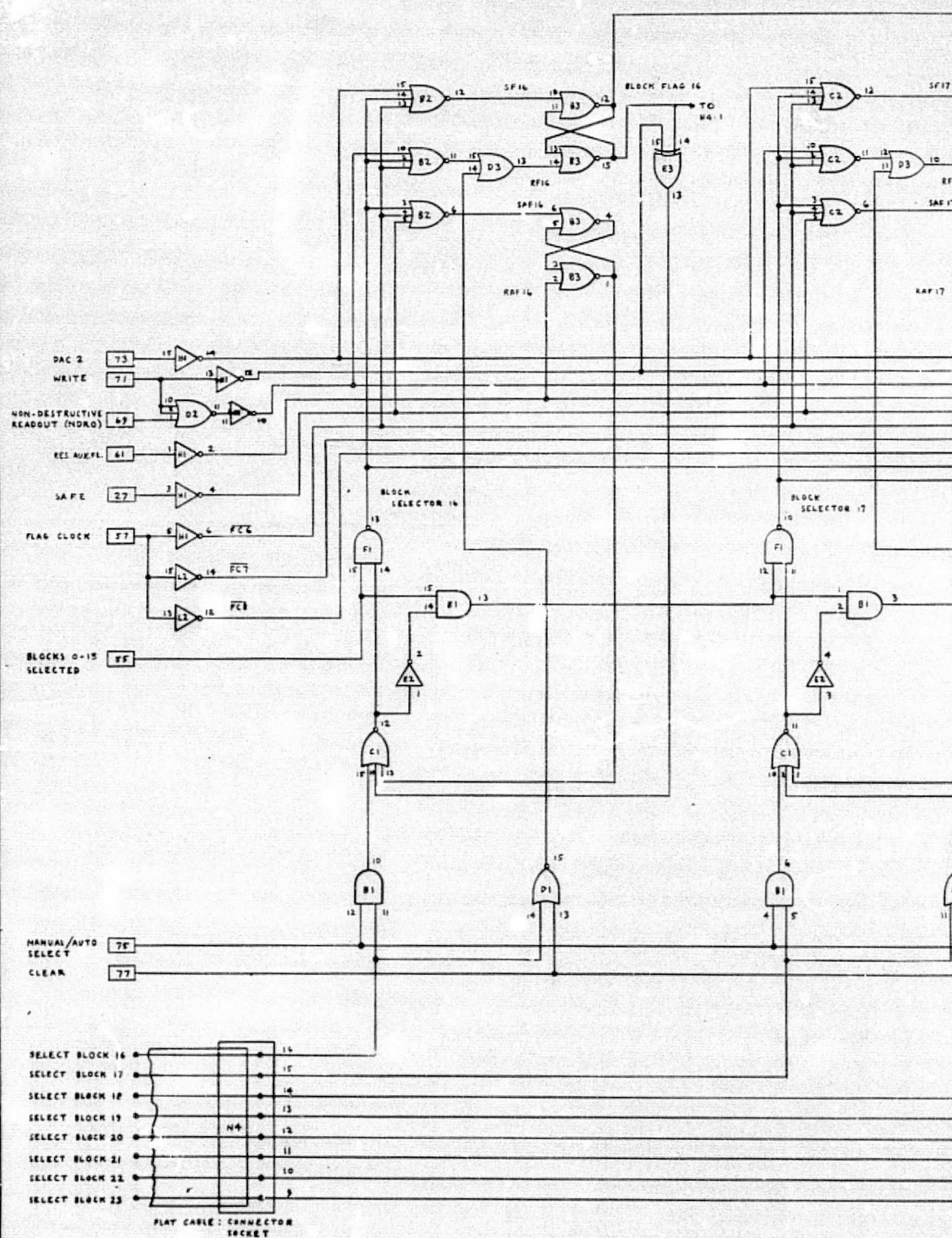




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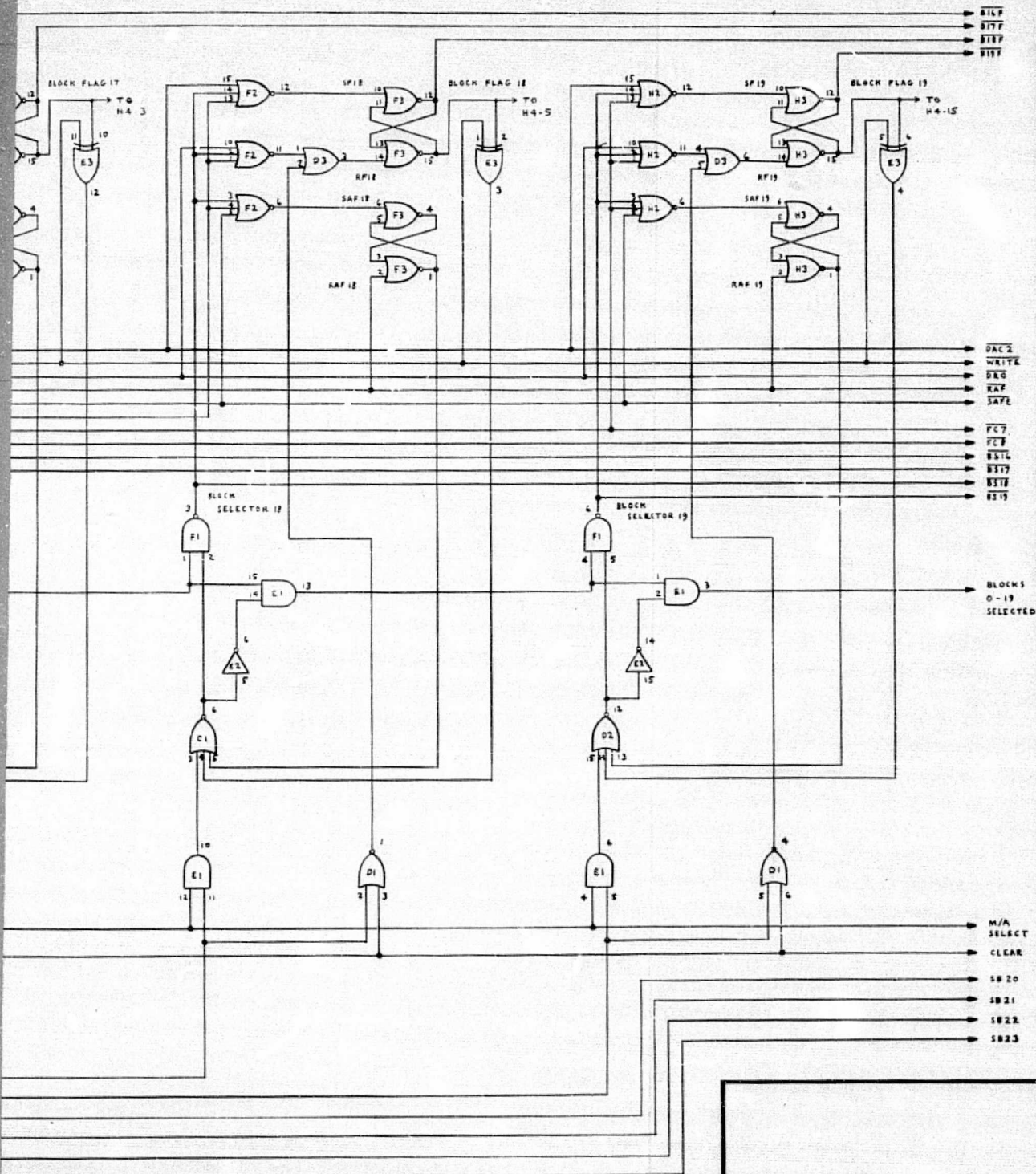
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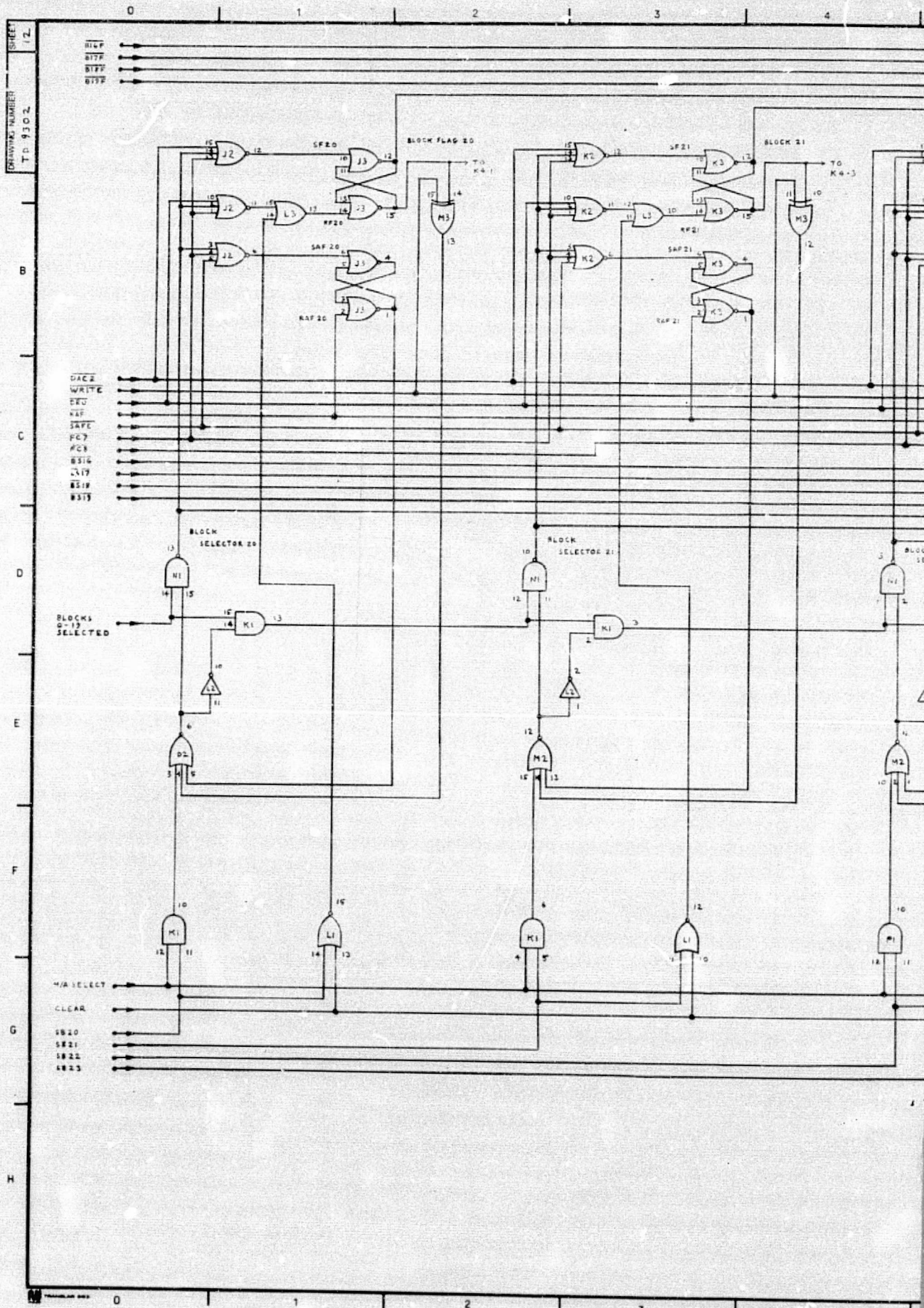
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ISSUE	AUTHORIZATION
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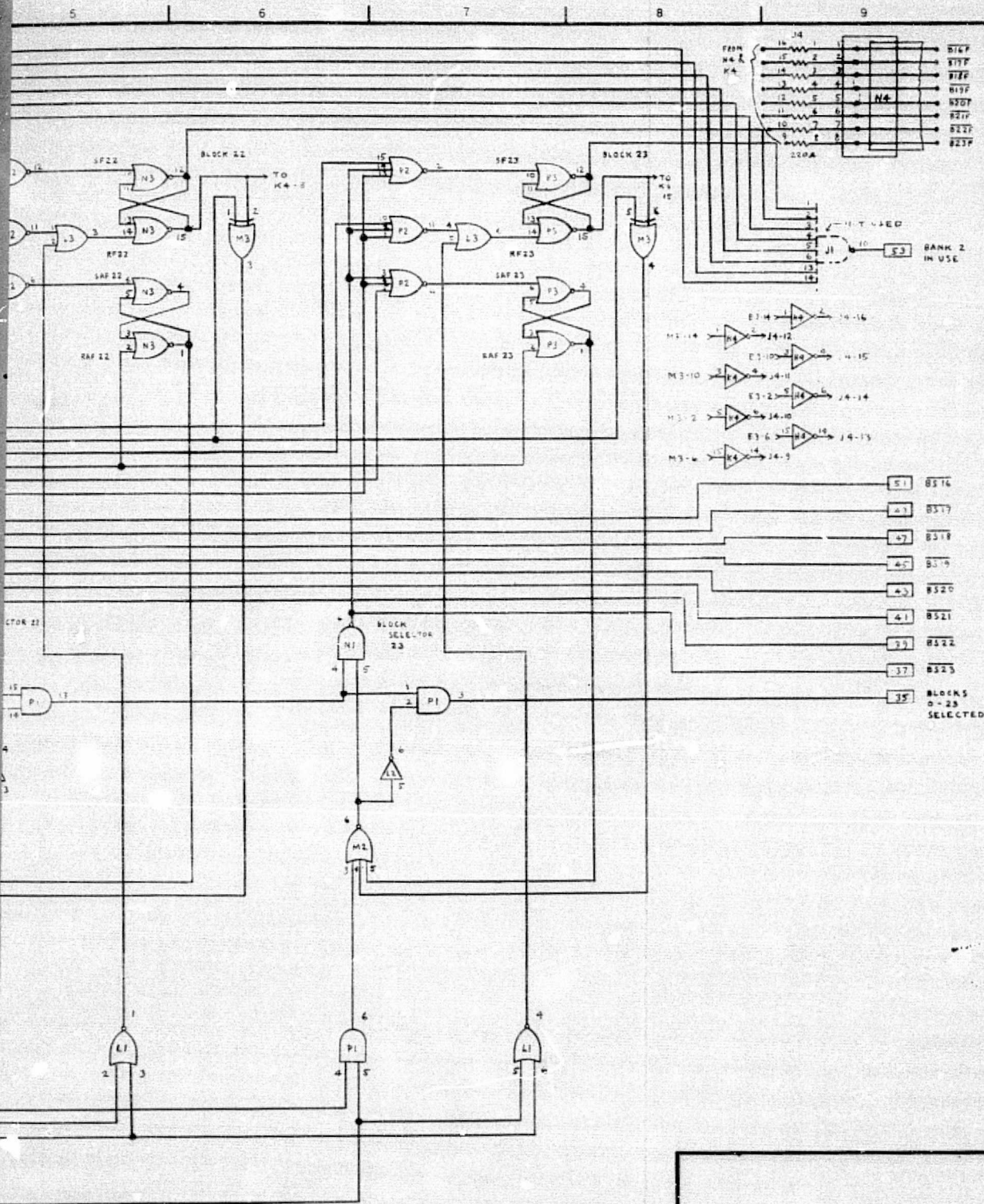
FOR IC LAYOUT,
SEE SHEET 7



TITLE		DESIGN AUTHORITY	
BLOCK SELECTOR AND BLOCK FLAGS FOR BLOCKS 16-19		Bell - Northern Research	
BOARD B		RATING	
Bell-Northern research		DRAWING NUMBER	
SIZE		TD 9302	
6S		SHEETS	
16		SHEET	
C-11		D100	

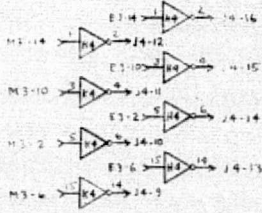
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ISSUE	AUTHORIZATION
3	K.4

FOR IC LAYOUT,
SEE SHEET 7.



- 51 B516
- 41 B517
- 47 B518
- 45 B519
- 43 B520
- 41 B521
- 39 B522
- 37 B523
- 35 BLOCKS 0-23 SELECTED

TITLE		DESIGN AUTHORITY	
BLOCK SELECTOR AND BLOCK FLAG FOR BLOCKS 20 TO 23		Bell-Northern Research	
BOARD 8		RATING	
		DRAWING NUMBER	
		TD 9302	
Bell-Northern research	SIZE	SHEETS	SHEET
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SHEET
13

DRAWING NUMBER
TD 9302

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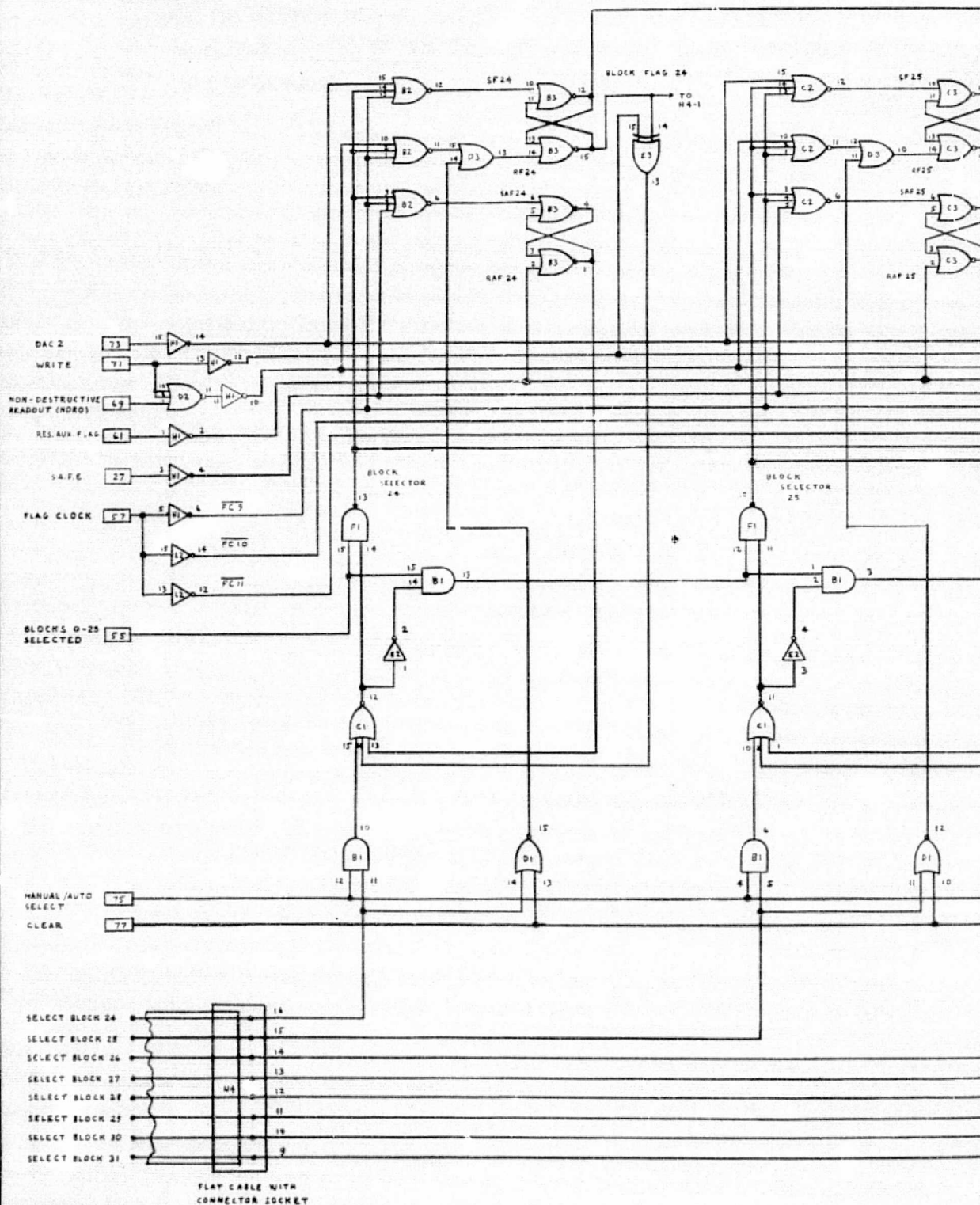
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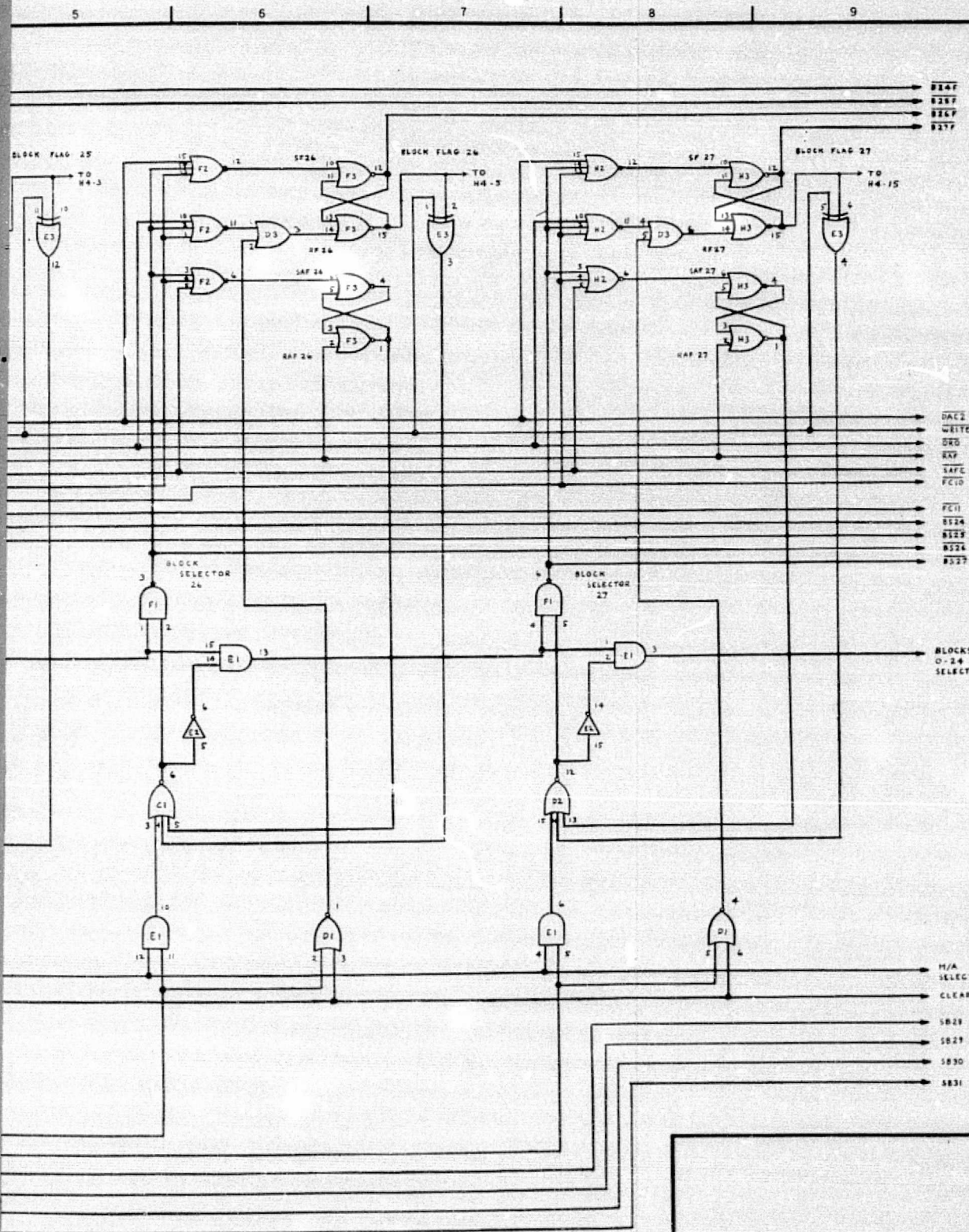
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FOR IC LAYOUT,
SEE SHEET 7

DATE
WRITE
DRG
REV
SAFE
FCID
FCID
ST24
ST29
ST26
ST27

BLOCKS
0-24
SELECTED

H/A
SELECT
CLEAR
SB28
SB29
SB30
SB31

TITLE
BLOCK SELECTOR AND
BLOCK FLAGS FOR
BLOCKS 24-27

BOARD A

DESIGN AUTHORITY Bell-Northern Research
RATING
DRAWING NUMBER TD 9302

Bell-Northern research



SIZE
6S

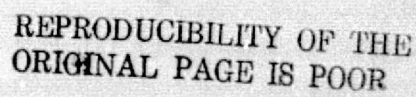
SHEETS
16

SHEET
C-13

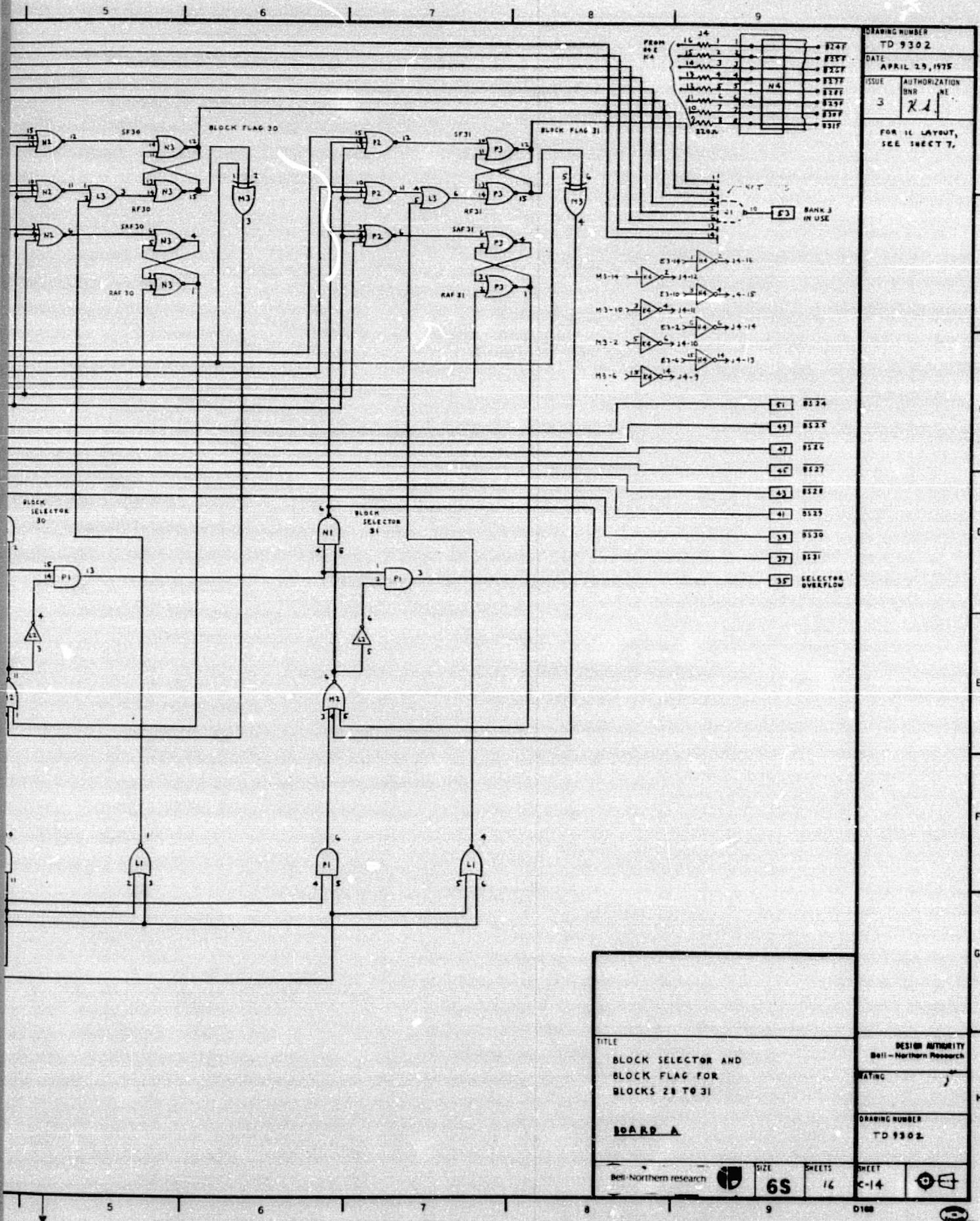


D100

DRAWING NUMBER	SHEET
TD 9302	14



REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR



DRAWING NUMBER	
TD 9302	
DATE	
APRIL 23, 1975	
ISSUE	AUTHORIZATION
3	21
FOR IL LAYOUT, SEE SHEET 7,	

TITLE		DESIGN AUTHORITY	
BLOCK SELECTOR AND BLOCK FLAG FOR BLOCKS 28 TO 31		Bell-Northern Research	
BOARD A		DRAWING NUMBER	
		TD 9302	
Bell-Northern Research	SIZE	SHEETS	SHEET
	6S	16	C-14

FOLDOUT FRAME

SHEET
15
DRAWING NUMBER
TO 9302

	A	B	C	D
	VCC	VCC	VCC	VCC
	2 1	2 1	2 1	2 1
	4 3	4 3	4 3	4 3
	6 5	6 5	6 5	6 5
	8 7	8 7	8 7	8 7
	10 9	10 9	10 9	10 9
	12 11	12 11	12 11	12 11
	14 13	14 13	14 13	14 13
	16 15	16 15	16 15	16 15
	18 17	18 17	18 17	18 17
	20 19	20 19	20 19	20 19
	22 21	22 21	22 21	22 21
	24 23	24 23	24 23	24 23
	26 25	26 25	26 25	26 25
	28 27	28 27	28 27	28 27
	30 29	30 29	30 29	30 29
	32 31	32 31	32 31	32 31
	34 33	34 33	34 33	34 33
	36 35	36 35	36 35	36 35
	38 37	38 37	38 37	38 37
	40 39	40 39	40 39	40 39
	42 41	42 41	42 41	42 41
	44 43	44 43	44 43	44 43
	46 45	46 45	46 45	46 45
	48 47	48 47	48 47	48 47
	50 49	50 49	50 49	50 49
	52 51	52 51	52 51	52 51
	54 53	54 53	54 53	54 53
	56 55	56 55	56 55	56 55
	58 57	58 57	58 57	58 57
	60 59	60 59	60 59	60 59
	62 61	62 61	62 61	62 61
	64 63	64 63	64 63	64 63
	66 65	66 65	66 65	66 65
	68 67	68 67	68 67	68 67
	70 69	70 69	70 69	70 69
	72 71	72 71	72 71	72 71
	74 73	74 73	74 73	74 73
	76 75	76 75	76 75	76 75
	78 77	78 77	78 77	78 77
	80 79	80 79	80 79	80 79
	82 81	82 81	82 81	82 81
	84 83	84 83	84 83	84 83
	86 85	86 85	86 85	86 85
	88 87	88 87	88 87	88 87
	90 89	90 89	90 89	90 89
	92 91	92 91	92 91	92 91
	94 93	94 93	94 93	94 93
	96 95	96 95	96 95	96 95
	98 97	98 97	98 97	98 97
	100 99	100 99	100 99	100 99
	102 101	102 101	102 101	102 101
	104 103	104 103	104 103	104 103
	106 105	106 105	106 105	106 105
	108 107	108 107	108 107	108 107
	110 109	110 109	110 109	110 109
	112 111	112 111	112 111	112 111
	114 113	114 113	114 113	114 113
	116 115	116 115	116 115	116 115
	118 117	118 117	118 117	118 117
	120 119	120 119	120 119	120 119
	GND	GND	GND	GND
	BLOCK SELECTOR AND BLOCK FLAGS 24-31	BLOCK SELECTOR AND BLOCK FLAGS 14-23	BLOCK SELECTOR AND BLOCK FLAGS 8-15	BLOCK SELECTOR AND BLOCK FLAGS 0-7

NOTES:

1. PINS LABELLED BA (EG BOARD 2, PIN 3) REFER TO BA (BLOCK ADDRESS) CONNECTOR ON THE REAR PANEL.
2. PINS LABELLED VAS (EG BOARD 2, PIN 31) REFER TO VAS (VA SELECT) CONNECTOR ON THE REAR PANEL.
3. PINS LABELLED TP (EG BOARD 2, PIN 11) REFER TO TEST POINT CONNECTOR ON THE REAR PANEL.

DRAWING NUMBER	
TD 9302	
DATE	
MAY 7, 1978	
ISSUE	AUTHORIZATION
3	KAL

E

F

H

J

VCC	2	1	VCC	2	1	VCC	2	1	VCC	2	1	VCC	2	1	VCC	2	1
(D51) 85G	4	3	NEXT (E149)	4	3	(E59) 85G	4	3	(E59) 85G	4	3	(E59) 85G	4	3	(E59) 85G	4	3
(D49) 85I	6	5	CE3 (H51, H51)	6	5	(E59) 85I	6	5	(E59) 85I	6	5	(E59) 85I	6	5	(E59) 85I	6	5
(D47) 85J	8	7	CE2 (H51, H51)	8	7	(E59) 85J	8	7	(E59) 85J	8	7	(E59) 85J	8	7	(E59) 85J	8	7
(D45) 85K	10	9	CE1 (H51, H51)	10	9	(E59) 85K	10	9	(E59) 85K	10	9	(E59) 85K	10	9	(E59) 85K	10	9
(D43) 85L	12	11	CE0 (H51, H51)	12	11	(E59) 85L	12	11	(E59) 85L	12	11	(E59) 85L	12	11	(E59) 85L	12	11
(D41) 85M	14	13	CEAT CE2 (H51)	14	13	(E59) 85M	14	13	(E59) 85M	14	13	(E59) 85M	14	13	(E59) 85M	14	13
(D39) 85N	16	15	CE3 (H51, H51)	16	15	(E59) 85N	16	15	(E59) 85N	16	15	(E59) 85N	16	15	(E59) 85N	16	15
(D37) 85P	18	17	CE2 (H51, H51)	18	17	(E59) 85P	18	17	(E59) 85P	18	17	(E59) 85P	18	17	(E59) 85P	18	17
(E51) 85Q	20	19	CE1 (H51, H51)	20	19	(E59) 85Q	20	19	(E59) 85Q	20	19	(E59) 85Q	20	19	(E59) 85Q	20	19
(E49) 85R	22	21	CE0 (H51, H51)	22	21	(E59) 85R	22	21	(E59) 85R	22	21	(E59) 85R	22	21	(E59) 85R	22	21
(E47) 85S	24	23	CE3 (H51)	24	23	(E59) 85S	24	23	(E59) 85S	24	23	(E59) 85S	24	23	(E59) 85S	24	23
(E45) 85T	26	25	CE2 (H51)	26	25	(E59) 85T	26	25	(E59) 85T	26	25	(E59) 85T	26	25	(E59) 85T	26	25
(E43) 85U	28	27	CE1 (H51)	28	27	(E59) 85U	28	27	(E59) 85U	28	27	(E59) 85U	28	27	(E59) 85U	28	27
(E41) 85V	30	29	CE0 (H51)	30	29	(E59) 85V	30	29	(E59) 85V	30	29	(E59) 85V	30	29	(E59) 85V	30	29
(E39) 85W	32	31	NEXT (E149)	32	31	(E59) 85W	32	31	(E59) 85W	32	31	(E59) 85W	32	31	(E59) 85W	32	31
(E37) 85X	34	33	CE3 (H51, H51)	34	33	(E59) 85X	34	33	(E59) 85X	34	33	(E59) 85X	34	33	(E59) 85X	34	33
(E35) 85Y	36	35	CE2 (H51, H51)	36	35	(E59) 85Y	36	35	(E59) 85Y	36	35	(E59) 85Y	36	35	(E59) 85Y	36	35
(E33) 85Z	38	37	CE1 (H51, H51)	38	37	(E59) 85Z	38	37	(E59) 85Z	38	37	(E59) 85Z	38	37	(E59) 85Z	38	37
(E31) 85A	40	39	CE0 (H51, H51)	40	39	(E59) 85A	40	39	(E59) 85A	40	39	(E59) 85A	40	39	(E59) 85A	40	39
(E29) 85B	42	41	NEXT (E149)	42	41	(E59) 85B	42	41	(E59) 85B	42	41	(E59) 85B	42	41	(E59) 85B	42	41
(E27) 85C	44	43	CE3 (H51)	44	43	(E59) 85C	44	43	(E59) 85C	44	43	(E59) 85C	44	43	(E59) 85C	44	43
(E25) 85D	46	45	CE2 (H51)	46	45	(E59) 85D	46	45	(E59) 85D	46	45	(E59) 85D	46	45	(E59) 85D	46	45
(E23) 85E	48	47	CE1 (H51)	48	47	(E59) 85E	48	47	(E59) 85E	48	47	(E59) 85E	48	47	(E59) 85E	48	47
(E21) 85F	50	49	CE0 (H51)	50	49	(E59) 85F	50	49	(E59) 85F	50	49	(E59) 85F	50	49	(E59) 85F	50	49
(E19) 85G	52	51	NEXT (E149)	52	51	(E59) 85G	52	51	(E59) 85G	52	51	(E59) 85G	52	51	(E59) 85G	52	51
(E17) 85H	54	53	CE3 (H51, H51)	54	53	(E59) 85H	54	53	(E59) 85H	54	53	(E59) 85H	54	53	(E59) 85H	54	53
(E15) 85I	56	55	CE2 (H51, H51)	56	55	(E59) 85I	56	55	(E59) 85I	56	55	(E59) 85I	56	55	(E59) 85I	56	55
(E13) 85J	58	57	CE1 (H51, H51)	58	57	(E59) 85J	58	57	(E59) 85J	58	57	(E59) 85J	58	57	(E59) 85J	58	57
(E11) 85K	60	59	CE0 (H51, H51)	60	59	(E59) 85K	60	59	(E59) 85K	60	59	(E59) 85K	60	59	(E59) 85K	60	59
(E09) 85L	62	61	NEXT (E149)	62	61	(E59) 85L	62	61	(E59) 85L	62	61	(E59) 85L	62	61	(E59) 85L	62	61
(E07) 85M	64	63	CE3 (H51)	64	63	(E59) 85M	64	63	(E59) 85M	64	63	(E59) 85M	64	63	(E59) 85M	64	63
(E05) 85N	66	65	CE2 (H51)	66	65	(E59) 85N	66	65	(E59) 85N	66	65	(E59) 85N	66	65	(E59) 85N	66	65
(E03) 85P	68	67	CE1 (H51)	68	67	(E59) 85P	68	67	(E59) 85P	68	67	(E59) 85P	68	67	(E59) 85P	68	67
(E01) 85Q	70	69	CE0 (H51)	70	69	(E59) 85Q	70	69	(E59) 85Q	70	69	(E59) 85Q	70	69	(E59) 85Q	70	69
(E59) 85R	72	71	NEXT (E149)	72	71	(E59) 85R	72	71	(E59) 85R	72	71	(E59) 85R	72	71	(E59) 85R	72	71
(E59) 85S	74	73	CE3 (H51, H51)	74	73	(E59) 85S	74	73	(E59) 85S	74	73	(E59) 85S	74	73	(E59) 85S	74	73
(E59) 85T	76	75	CE2 (H51, H51)	76	75	(E59) 85T	76	75	(E59) 85T	76	75	(E59) 85T	76	75	(E59) 85T	76	75
(E59) 85U	78	77	CE1 (H51, H51)	78	77	(E59) 85U	78	77	(E59) 85U	78	77	(E59) 85U	78	77	(E59) 85U	78	77
(E59) 85V	80	79	CE0 (H51, H51)	80	79	(E59) 85V	80	79	(E59) 85V	80	79	(E59) 85V	80	79	(E59) 85V	80	79
(E59) 85W	82	81	NEXT (E149)	82	81	(E59) 85W	82	81	(E59) 85W	82	81	(E59) 85W	82	81	(E59) 85W	82	81
(E59) 85X	84	83	CE3 (H51)	84	83	(E59) 85X	84	83	(E59) 85X	84	83	(E59) 85X	84	83	(E59) 85X	84	83
(E59) 85Y	86	85	CE2 (H51)	86	85	(E59) 85Y	86	85	(E59) 85Y	86	85	(E59) 85Y	86	85	(E59) 85Y	86	85
(E59) 85Z	88	87	CE1 (H51)	88	87	(E59) 85Z	88	87	(E59) 85Z	88	87	(E59) 85Z	88	87	(E59) 85Z	88	87
(E59) 85A	90	89	CE0 (H51)	90	89	(E59) 85A	90	89	(E59) 85A	90	89	(E59) 85A	90	89	(E59) 85A	90	89
(E59) 85B	92	91	NEXT (E149)	92	91	(E59) 85B	92	91	(E59) 85B	92	91	(E59) 85B	92	91	(E59) 85B	92	91
(E59) 85C	94	93	CE3 (H51, H51)	94	93	(E59) 85C	94	93	(E59) 85C	94	93	(E59) 85C	94	93	(E59) 85C	94	93
(E59) 85D	96	95	CE2 (H51, H51)	96	95	(E59) 85D	96	95	(E59) 85D	96	95	(E59) 85D	96	95	(E59) 85D	96	95
(E59) 85E	98	97	CE1 (H51, H51)	98	97	(E59) 85E	98	97	(E59) 85E	98	97	(E59) 85E	98	97	(E59) 85E	98	97
(E59) 85F	100	99	CE0 (H51, H51)	100	99	(E59) 85F	100	99	(E59) 85F	100	99	(E59) 85F	100	99	(E59) 85F	100	99
(E59) 85G	102	101	NEXT (E149)	102	101	(E59) 85G	102	101	(E59) 85G	102	101	(E59) 85G	102	101	(E59) 85G	102	101
(E59) 85H	104	103	CE3 (H51, H51)	104	103	(E59) 85H	104	103	(E59) 85H	104	103	(E59) 85H	104	103	(E59) 85H	104	103
(E59) 85I	106	105	CE2 (H51, H51)	106	105	(E59) 85I	106	105	(E59) 85I	106	105	(E59) 85I	106	105	(E59) 85I	106	105
(E59) 85J	108	107	CE1 (H51, H51)	108	107	(E59) 85J	108	107	(E59) 85J	108	107	(E59) 85J	108	107	(E59) 85J	108	107
(E59) 85K	110	109	CE0 (H51, H51)	110	109	(E59) 85K	110	109	(E59) 85K	110	109	(E59) 85K	110	109	(E59) 85K	110	109
(E59) 85L	112	111	NEXT (E149)	112	111	(E59) 85L	112	111	(E59) 85L	112	111	(E59) 85L	112	111	(E59) 85L	112	111
(E59) 85M	114	113	CE3 (H51)	114	113	(E59) 85M	114	113	(E59) 85M	114	113	(E59) 85M	114	113	(E59) 85M	114	113
(E59) 85N	116	115	CE2 (H51)	116	115	(E59) 85N	116	115	(E59) 85N	116	115	(E59) 85N	116	115	(E59) 85N	116	115
(E59) 85P	118	117	CE1 (H51)	118	117	(E59) 85P	118	117	(E59) 85P	118	117	(E59) 85P	118	117	(E59) 85P	118	117
(E59) 85Q	120	119	CE0 (H51)	120	119	(E59) 85Q	120	119	(E59) 85Q	120	119	(E59) 85Q	120	119	(E59) 85Q	120	119

ADDRESS
CONTROLS
AND
DATA
OUTPUT

128 K-BIT
CCD
MEMORY

CCD CLOCKS
AND
TIMING CONTROLS

DATA
INPUT
BUFFER

TITLE		DESIGN AUTHORITY	
EDGE CONNECTOR PINOUTS		Bell - Northern Research	
RATING		DRAWING NUMBER	
		TD 9302	
Bell-Northern research	SIZE	SHEETS	SHEET
	6S	16	C-15

CONNECTION NUMBER
TD 9302

B

C

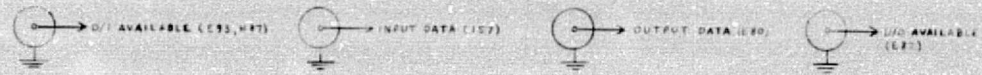
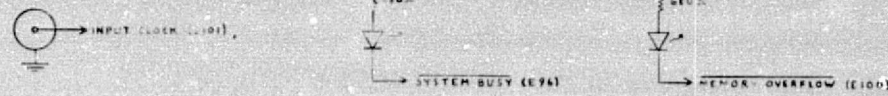
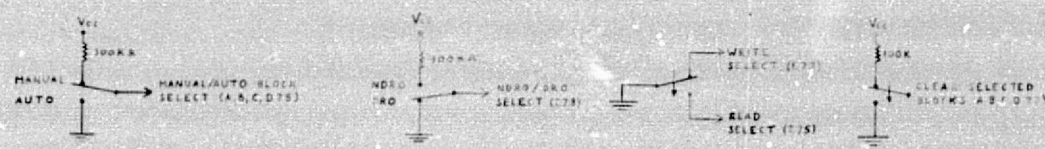
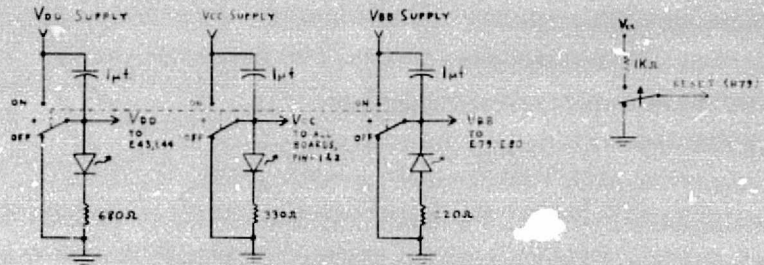
D

E

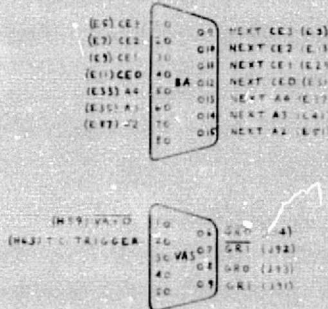
F

G

H



FRONT PANEL SCHEMATIC

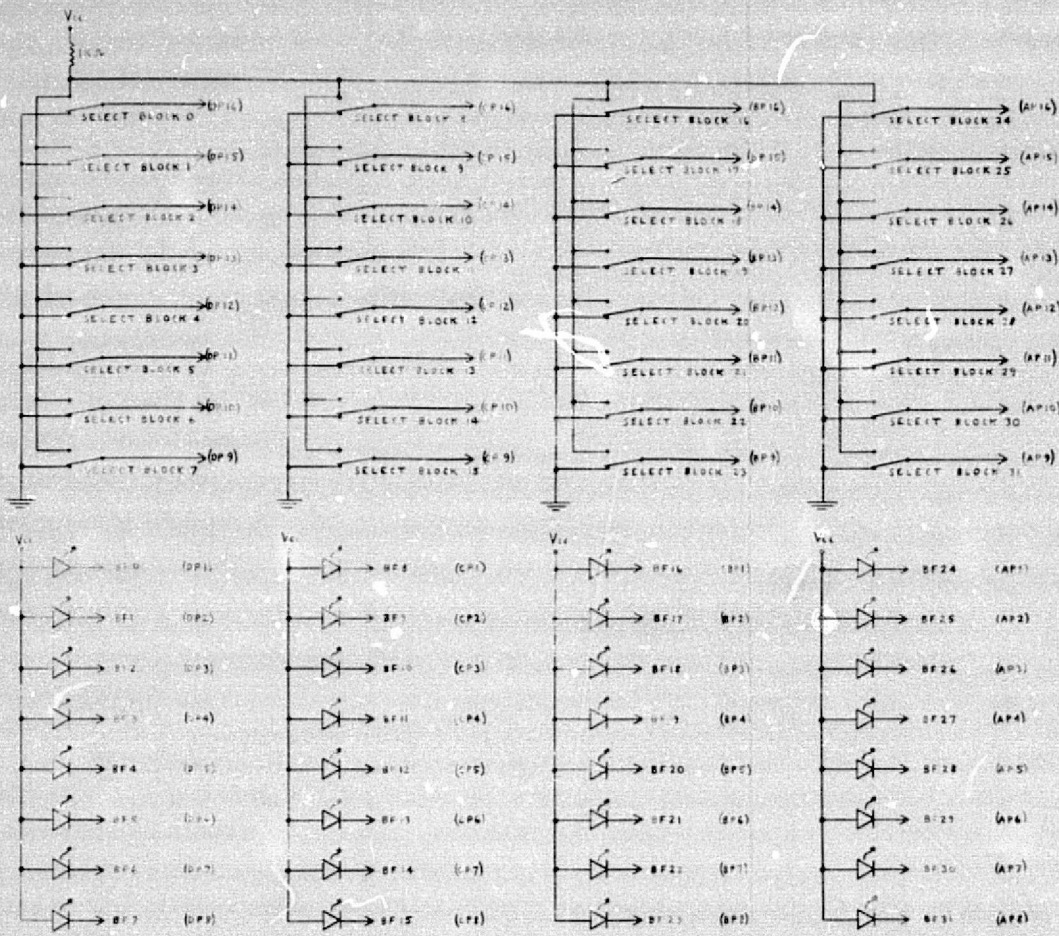


TFA

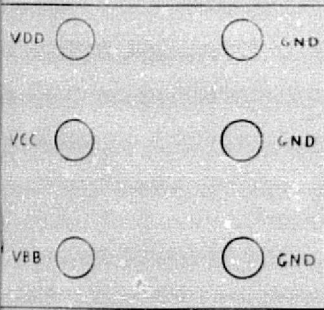
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8	7	1	171
10	9	1	167
12	11	1	167
14	13	1	165
16	15	1	163
18	17	1	161
20	19	1	159
22	21	1	155
24	23	1	149
26	25	1	145
28	27	1	143
30	29	1	141
32	31	1	139
34	33	1	137
36	35	1	135
38	37	1	133
40	39	1	131
42	41	1	129
44	43	1	127

BACK PANEL SCHEMATIC

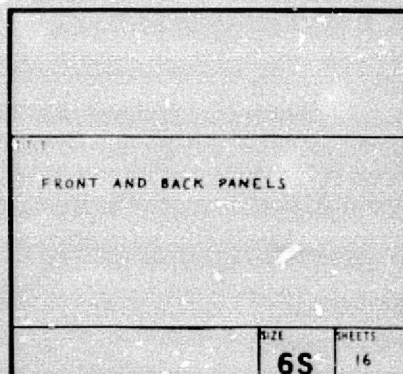
FOLDOUT FRAME 2



NOTE: ABOVE PIN CONNECTIONS REFER TO PANEL CONNECTOR SOCKET CORRESPONDING TO EACH PANEL.



POWER SUPPLY CONNECTOR PANEL



FRONT AND BACK PANELS

DRAWN: NUB...	
TD 9302	
DATE	
FEB. 1, 1976	
ISSUE	AUTHORIZATION
3	NR ME
NOTES:	
ALL LED'S EXCEPT NUMERICAL READOUTS ARE MV5022.	
A	
B	
C	
D	
E	
F	
G	
H	
DESIGN AUTHORITY	
Bell-Northern Research	
RATING	
DRAWING NUMBER	
TD 9302	
SIZE	SHEETS
6S	16
SHEET	C-16
D100	

List of Symbols on SchematicsSheet 1

DAC 1	Data Available Control 1
DAC 1 (MOD)	DAC1 (modified)
GRO / GR1	Gray code counter bits
GR0L / GR1L	Gray code counter bits - latched
RAM WE PULSE	RAM write enable pulse
RAM ADD. Qn	RAM address bit Qn

Sheet 2

RAQn	RAM Address bit Qn
DI CCD n	Data input to CCD n

Sheet 3

CE n	Chip Enable n
TC trigger	Timing Chain Trigger
VA = 0	Virtual Address = 0
VA = X00	Virtual Address = X00
$\emptyset_{x,y}$	CCD clock x to bank y

Sheet 4

DIn	CCD data input n
W	Write
An	CCD track addresses
DOn	CCD Data output n

A P P E N D I X D

Specifications for INS4200 RAM

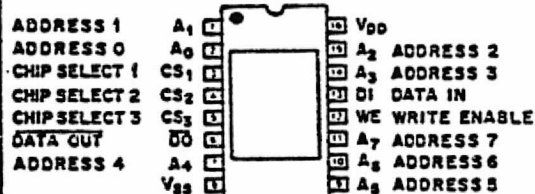
ADVANCE INFORMATION

- *CMOS: 5-15V Supply Range*
- **Low Power Dissipation**
40 μ W Standby
26mW Operating
- **High Speed**
180nS Read Cycle
140nS Write Cycle
- **Static Operation**
- **256 Word X 1 Bit Organization**
- **Three-State TTL Compatible Output**
- **Full Address Decoding**
- **Bipolar Compatible Pin-Outs**
- **16 Pin Package**

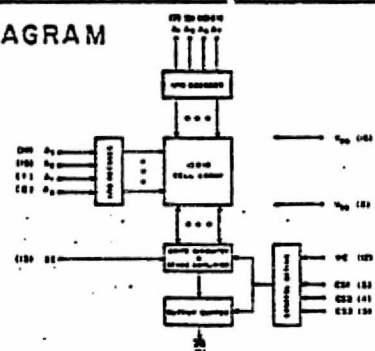
GENERAL DESCRIPTION

The Inselek INS4200S is a low power 256WX1B memory constructed with SOS/CMOS (Silicon-on-Sapphire/Complementary Metal-Oxide-Semiconductor) process. It is fully compatible with other INS4000S components as well as other CMOS and TTL devices. It is intended for use in scratch pad, buffer and main memory applications where high speed and low power are required. Like its TTL counterparts, the INS4200S can tolerate successive address changes during the Read Cycle while the Chip Select remains enabled.

PIN CONFIGURATION



BLOCK DIAGRAM

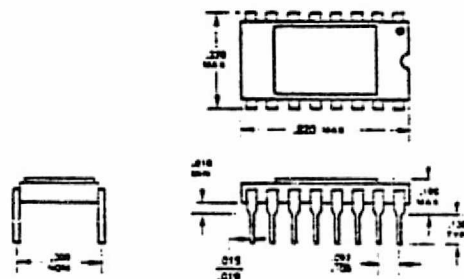


TRUTH TABLE

INPUTS					OUTPUT	MODE
CS ₁	CS ₂	CS ₃	WE	DI	DO	
H	X	X	X	X	Floats	UNSELECTED
X	H	X	X	X	Floats	
X	X	H	X	X	Floats	
L	L	L	L	L	H	Write
L	L	L	L	H	L	Write
L	L	L	H	X	High/L	Read

H=High Voltage (V_{DD}); L=Low Voltage (V_{SS}); X=Can't Care

PACKAGE OUTLINE



ABSOLUTE MAXIMUM RATINGS

INS4200S

Operating Temperature

$T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Storage Temperature

$T_A = -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

Supply Voltage

$V_{DD} - V_{SS} = +15\text{V}$

Input Voltage

$V_{IN} = V_{DD}$ to V_{SS}

RECOMMENDED SUPPLY VOLTAGE

$5.0\text{V} \leq V_{DD} - V_{SS} \leq 15.0\text{V}$

D.C. CHARACTERISTICS

$V_{SS} = 0$

SYMBOL	PARAMETERS	DESIGN OBJECTIVES									UNITS	TEST CONDITIONS
		-55°C			+25°C			+125°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V _{OL}	Output Low Voltage			0.01		0	0.01			0.05	V	V _{IN} = V _{DD} = 5V
				0.01		0	0.01			0.05	V	V _{IN} = V _{DD} = 10V
V _{OH}	Output High Voltage	4.99			4.99	5		4.95			V	V _{IN} = 0V, V _{DD} = 5V
		9.99			9.99	10		9.95			V	V _{IN} = 0V, V _{DD} = 10V
V _{NL} *	Noise Immunity	1.5			1.5	2.25		1.4			V	V _{OUT} = 3.5V, V _{DD} = 5V
		3.0			3.0	4.5		2.9			V	V _{OUT} = 7.0V, V _{DD} = 10V
V _{NH} *	Noise Immunity	1.4			1.5	2.25		1.5			V	V _{OUT} = 1.5V, V _{DD} = 5V
		2.9			3.0	4.5		3.0			V	V _{OUT} = 3.0V, V _{DD} = 10V
I _{OL}	Output Drive	2.0			1.6	2.0		1.1			mA	V _{OUT} = 0.5V, V _{DD} = 5V
	Current	5.0			4.0	5.0		2.8			mA	V _{OUT} = 0.5V, V _{DD} = 10V.
I _{OH}	Output Drive	0.6			0.5	2.5		0.3			mA	V _{OUT} = 2.5V, V _{DD} = 5V
	Current	0.6			0.5	2.2		0.3			mA	V _{OUT} = 9.5V, V _{DD} = 10V
C _{IN}	Input Capacitance					6.5					pF	
P _{DS}	Quiescent Power					5	125				μW	V _{DD} = 5V, CS ₁ = 5V
	Dissipation (Standby)					10	250				μW	V _{DD} = 10V, CS ₁ = 10V
P _{DC}	Operating Power					10	20				mW	V _{DD} = 5V, CS ₁ -CS ₂ -CS ₃ =0V
	Dissipation					20	40				mW	V _{DD} =10V, CS ₁ -CS ₂ -CS ₃ =0V

*Maximum input voltage deviation from an ideal logic "1" or "0" level beyond which output changes state.

SWITCHING CHARACTERISTICS: $V_{DD} = 10\text{V}, V_{SS} = 0, T_A = 25^{\circ}\text{C}, C_L = 15\text{pF}$

SYMBOL	PARAMETERS	DESIGN OBJECTIVES			UNITS
		MIN.	TYP.	MAX.	
t_{AC}	Minimum Address to Chip Select Delay		20	30	nS
t_{A1}^*	Access Time: Chip Select to Output Delay		160	240	nS
t_{A2}^*	Access Time: Address to Output Delay		160	270	nS
t_{OR}	Output Recovery Time		45	70	nS
t_{CA}	Minimum Chip Select Removal to Address Delay		10	15	nS
t_{AA}	Minimum Address to Address Delay		140	225	nS
t_{AW}	Minimum Address to Write Enable Delay		20	30	nS
t_{WP}	Time to Complete Write Operation		40	60	nS
t_{WA}	Minimum Write Enable Removal to Address Delay		80	125	nS

*Accessed data is valid only when both t_{A1} and t_{A2} are satisfied.

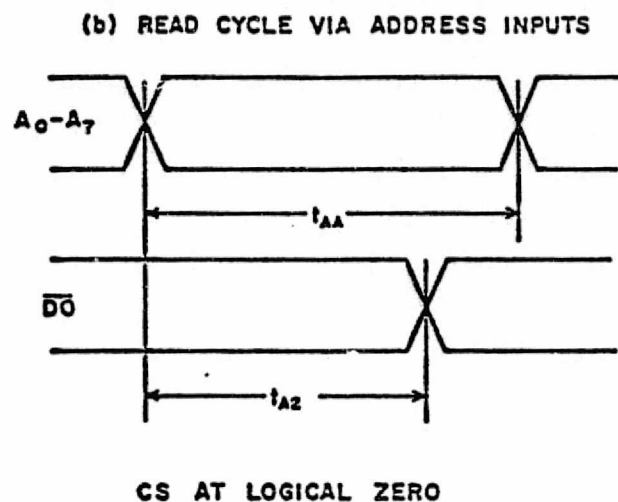
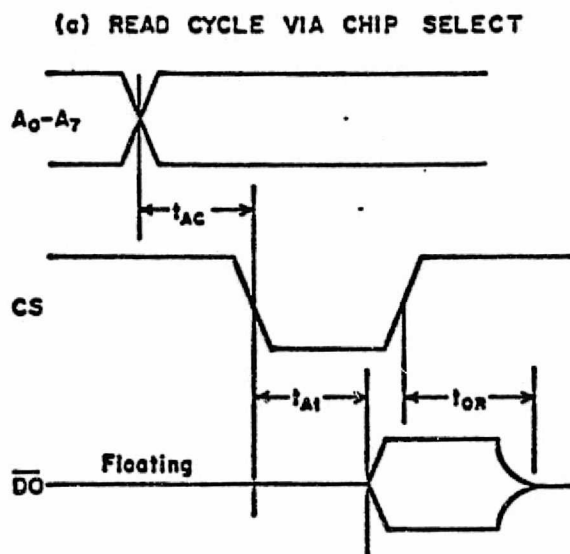


FIGURE 1. READ CYCLE TIMING DIAGRAMS

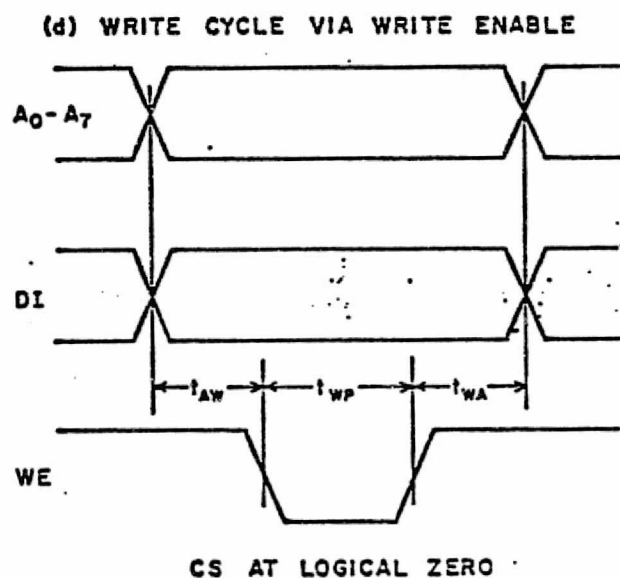
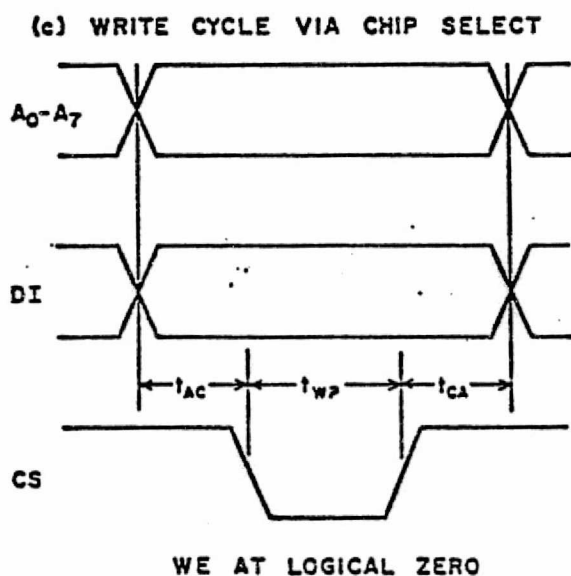


FIGURE 2. WRITE CYCLE TIMING DIAGRAMS

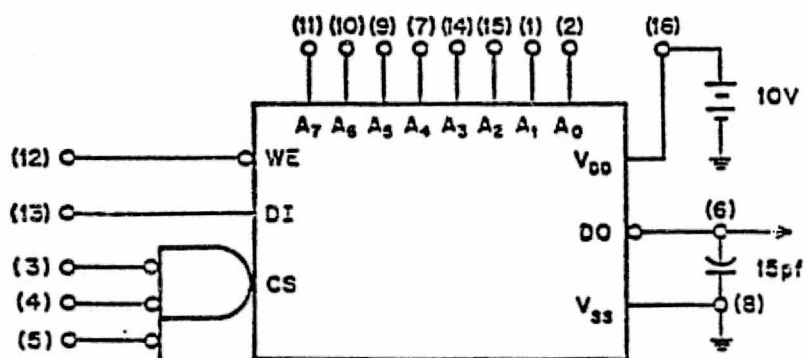
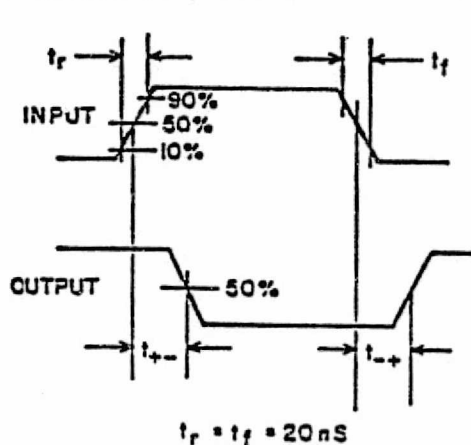


FIGURE 3. TEST CONFIGURATION & WAVEFORMS

A P P E N D I X E

Specifications for MH0026 Clock Driver



Memory/Clock Drivers

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled: i.e., the output pulse width is equal to the input pulse width.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive— ± 1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load

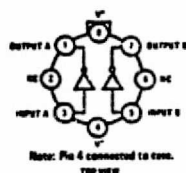
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the application section starting on page 5. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

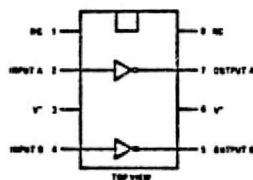
connection diagrams

Metal Can Package



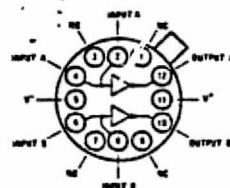
Order Number MH0026H
or MH0026CH
See Package 11

Dual-In-Line Package



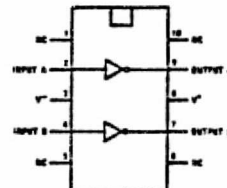
Order Number MH0026CN
See Package 20

Metal Can Package



Order Number MH0026G
or MH0026CG
See Package 6

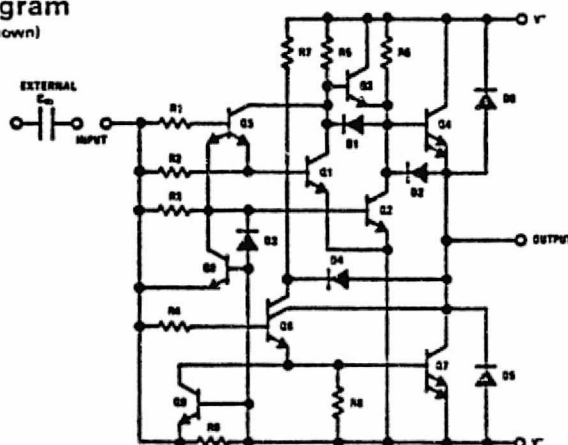
Flat Package



Order Number MH0026F
or MH0026CF
See Package 3

schematic diagram

(1/2 of Circuit Shown)



absolute maximum ratings

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Power Dissipation	See curves
Operating Temperature Range	MH0026 -55°C to +125°C
	MH0026C 0°C to 85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Notes 1 & 2)

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V, V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V, V_{OUT} = V^+ - 1.0V$		-0.005	-10	μA
Logic "0" Output Voltage	$V^+ = +5.0V, V^- = -12.0V$ $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V, V^- = -12.0V$ $V_{IN} = -9.5V$		-11.5	-11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V, V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V, V_{IN} - V^- = 0.0V$		10	100	μA

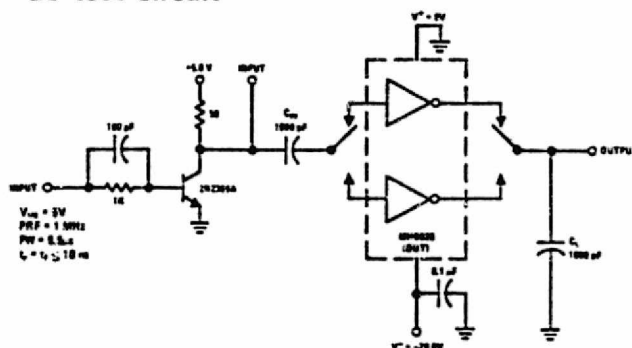
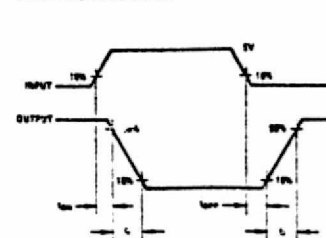
ac electrical characteristics (Notes 1 & 2, AC test circuit, $T_A = 25^\circ C$)

Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) - Note 3	$V^+ - V^- = 17V, C_L = 250 pF$		12		ns
	$V^+ - V^- = 17V, C_L = 500 pF$		15	18	ns
	$C_L = 1000 pF$		20	35	ns
Falltime (t_f) - Note 3	$V^+ - V^- = 17V, C_L = 250 pF$		10		ns
	$V^+ - V^- = 17V, C_L = 500 pF$		12	16	ns
	$C_L = 1000 pF$		17	25	ns

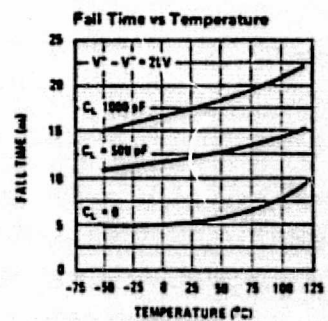
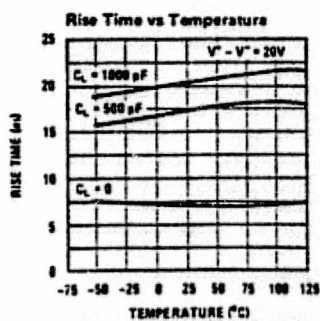
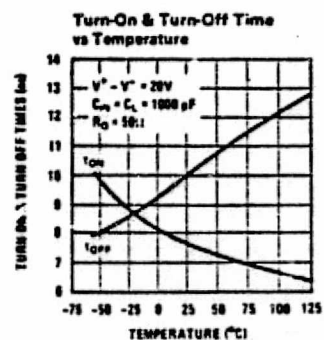
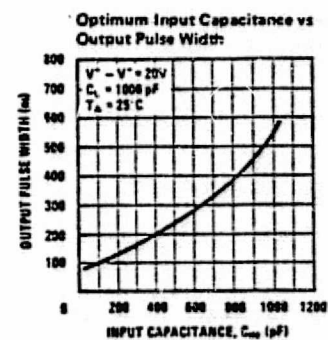
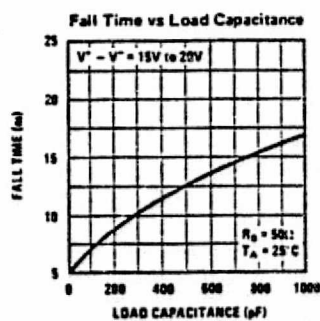
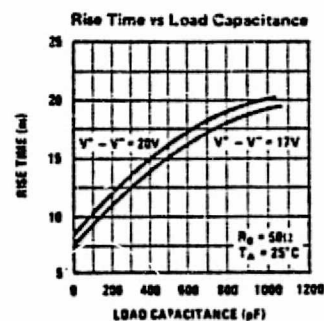
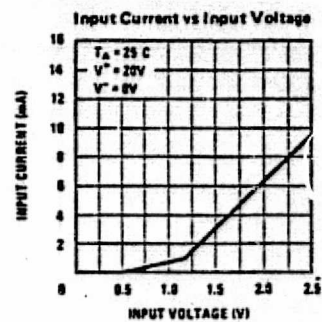
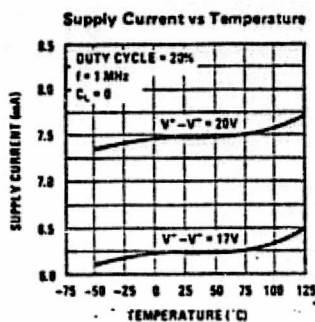
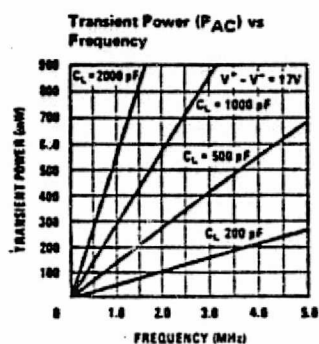
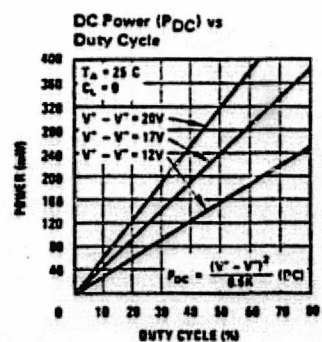
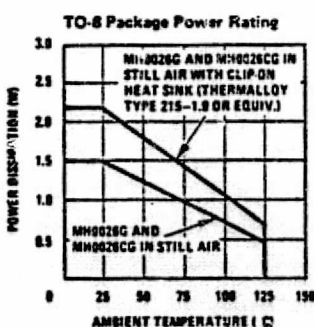
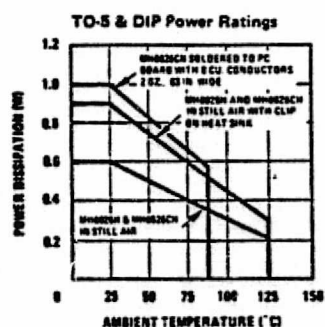
Note 1: These specifications apply for $V^+ - V^- = 10V$ to $20V$, $C_L = 1000 pF$, over the temperature range $-55^\circ C$ to $+125^\circ C$ for the MH0026 and $0^\circ C$ to $+85^\circ C$ for the MH0026C, unless otherwise specified.

Note 2: All typical values for the $T_A = 25^\circ C$.

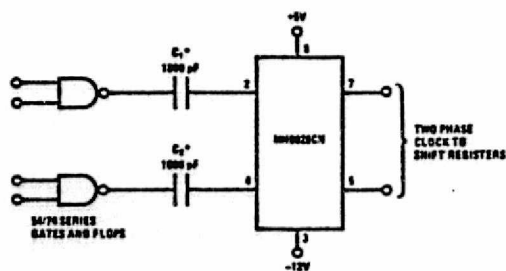
Note 3: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See waveforms on the following pages.

ac test circuit**switching time waveforms**

typical performance characteristics

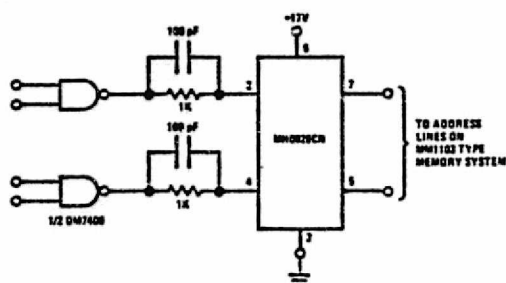


AC Coupled MOS Clock Driver

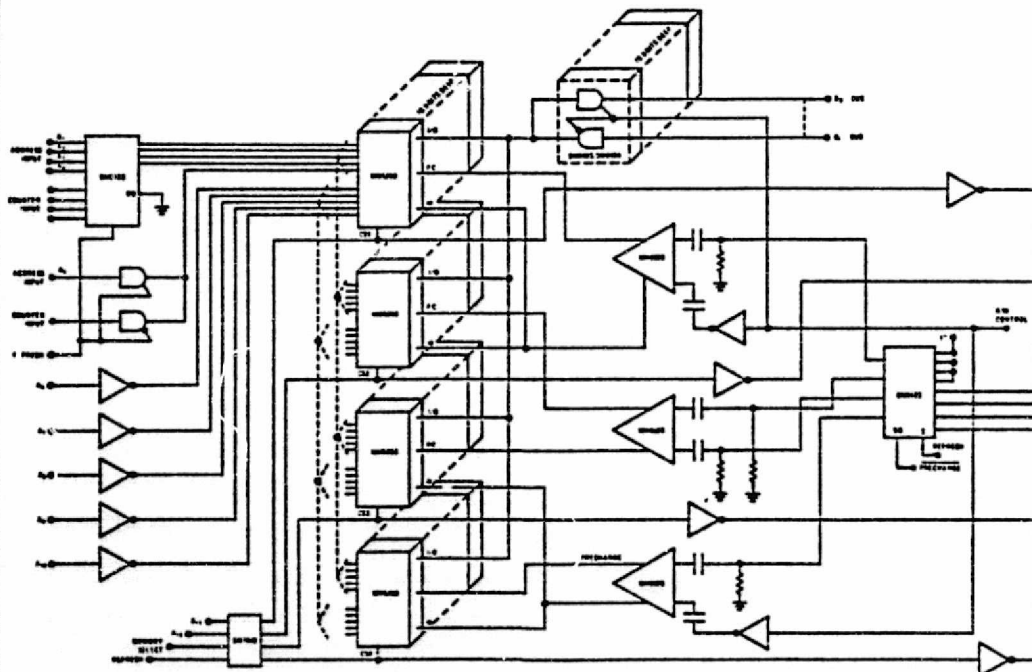


*See applications section for detailed information on input/output design criteria.

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

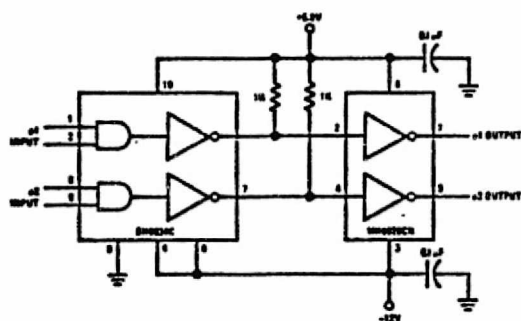


Precharge Driver for MOS RAM Memories

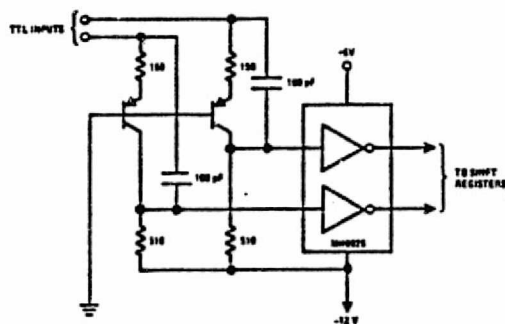


typical applications

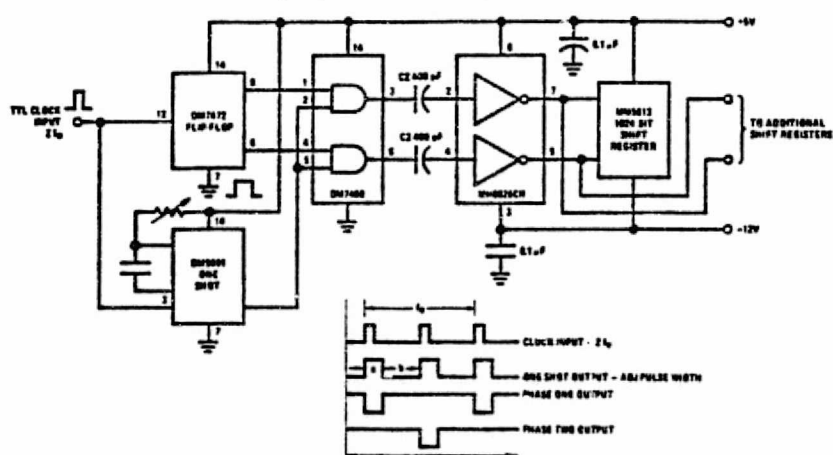
DC Coupled MOS Clock Driver



Transistor Coupled MOS Clock Driver



Logically Controlled AC Coupled Clock Driver



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitive loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide range of supplies while the output pulse width may be controlled by the time constant $-R_1 \times C_1$.

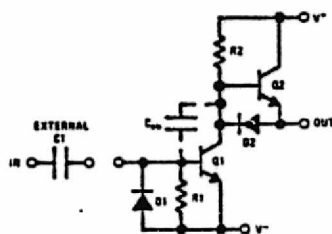


FIGURE 1. Conventional MOS Clock Drive

Q_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1 , both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

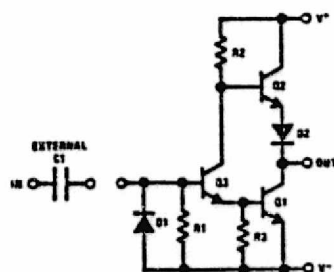


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these classic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 2µs rise and fall times into 1000pF loads. In

a simplified diagram, Q_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. Q_2 prevents zenering of the emitter-base junction of Q_3 and provides an initial discharge path for the load via Q_3 . During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4 .

The complete circuit of the MH0026 (see schematic on page 1) basically makes Darlington's out of each of the transistors in Figure 3.

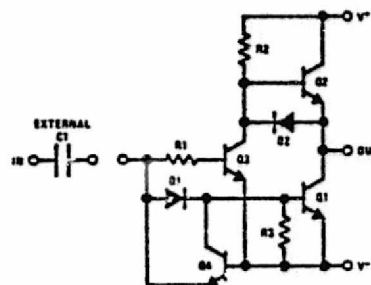


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reach 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by Q_1 and Q_2 . When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7 . As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_6 and Q_7 to conduct momentarily to assure rapid turn-off of Q_3 and Q_4 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts. R_6 assures that the output will reach to within one V_{BE} of the V^+ supply.

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_6 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

application information (cont.)

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually negligible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per drive):

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times \left(\frac{\text{ON time}}{\text{OFF time} + \text{ON time}} \right)$$

or $P_{DC} = (\text{Output Low Power}) \times (\text{Duty Cycle})$

where: $I_{S(Low)} = I_S @ (V^+ - V^-)$

Example 1: ($V^+ = +5V$, $V^- = -12V$)

a) Duty cycle = 25%, therefore

$$P_{DC} = 17V \times 40mA \times 17/20 \times 25\%$$

$$P_{DC} = 145mW \text{ worst-case, each side}$$

$$P_{DC} = 109mW \text{ typically}$$

b) Duty cycle = 5%

$$P_{DC} = 21mW$$

c) See graph on page 3

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: ($V^+ = +17V$, $V^- = GND$):

a) Duty cycle = 50%

$$P_{DC} = 290mW \text{ worst-case}$$

$$P_{DC} = 218mW \text{ typically}$$

b) Duty cycle = 100%

$$P_{DC} = 580mW$$

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: ($V^+ = +5V$, $V^- = -12V$)

$$P_{AC} = 17 \times 17 \times f(\text{MHz}) \times 10^6 \times$$

$$C_L(\text{nF}) \times 10^{-9}$$

$$P_{AC} = 290mW \text{ per MHz per } 1000pF$$

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs on page 3 illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent—derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

application information (cont.)

3.4 Summary—Package Power Considerations

The maximum capacitive load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{\text{max(mw)}}(T_A, \text{pkg}) \times R_{\text{eq}} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times R_{\text{eq}} \times f(\text{MHz})}$$

$$\text{or: } C_L \text{ (max in pF)} = 5 \times 10^{-3} \times \frac{P_{\text{max(mw)}} \times 500 - V_S^2 \times Dc \times 10^3}{V_S^2 \times 500 \times f(\text{MHz})}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{\text{max(mw)}}(T_A, \text{pkg})$ = Package power rating in milliwatts for given package, heat sink, and max. ambient temperature (See graphs)

R_{eq} = equivalent internal resistance

$R_{\text{eq}} = (V^+ - V^-) / I_{S(\text{Low})} = 500 \text{ ohms (worst case over temperature for the MH0026 or 660 ohms typically)}$

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low} + \text{Time in output high state}}$$

Table 1 illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{\text{OUT}} = (PW)_{\text{IN}} + \frac{t_r + t_f}{2} = PW_{\text{IN}} + 25\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_r will be degraded. The graph on page 3 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{\text{IN}} = (2 \times 10^{-3}) (PW)_{\text{OUT}}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{\text{IN}} = (2 \times 10^{-3}) (500 \times 10^{-9}) \cong 1000\text{pF}$$

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency	Max. Ambient Temp. → Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	—	—

*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\text{V}$. For loads greater than 1200 pF, rise and fall times will be limited by output current; see Section 5.9

application information (cont.)

5.0 Rise & Fall Time Considerations (Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} < 1.5A$$

The rise time, t_r , for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12}) \\ = 25ns$$

For small values of C_L , equation above predicts optimistic values for t_r . The graph on page 3 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R(C_S + C_L) \\ h_{FE} + 1$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the MH0026. The critical value for $R_s = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In

practice, determination of a value for L is rather difficult. However, R_s is readily determined empirically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2R_s C_L$$

7.0 Clock Line Cross Talk

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2 , the output has to drop at least $2V_{be}$ before Q_3 and Q_4 come on and pull the output back to V^+ . A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4 . When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{FE} . The spike is quickly clamped by Q_4 . Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

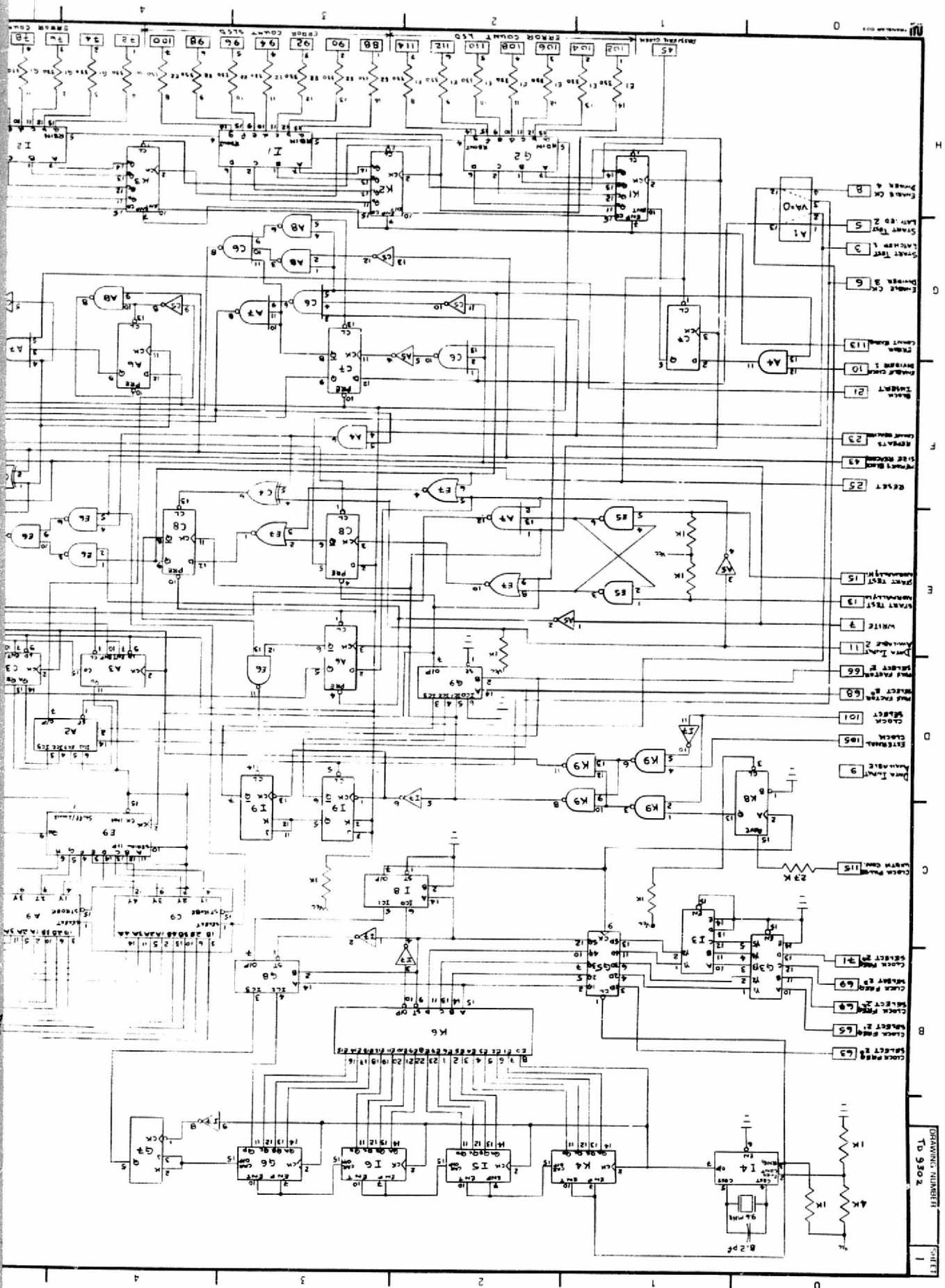
8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least $0.1\mu F$ noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

3

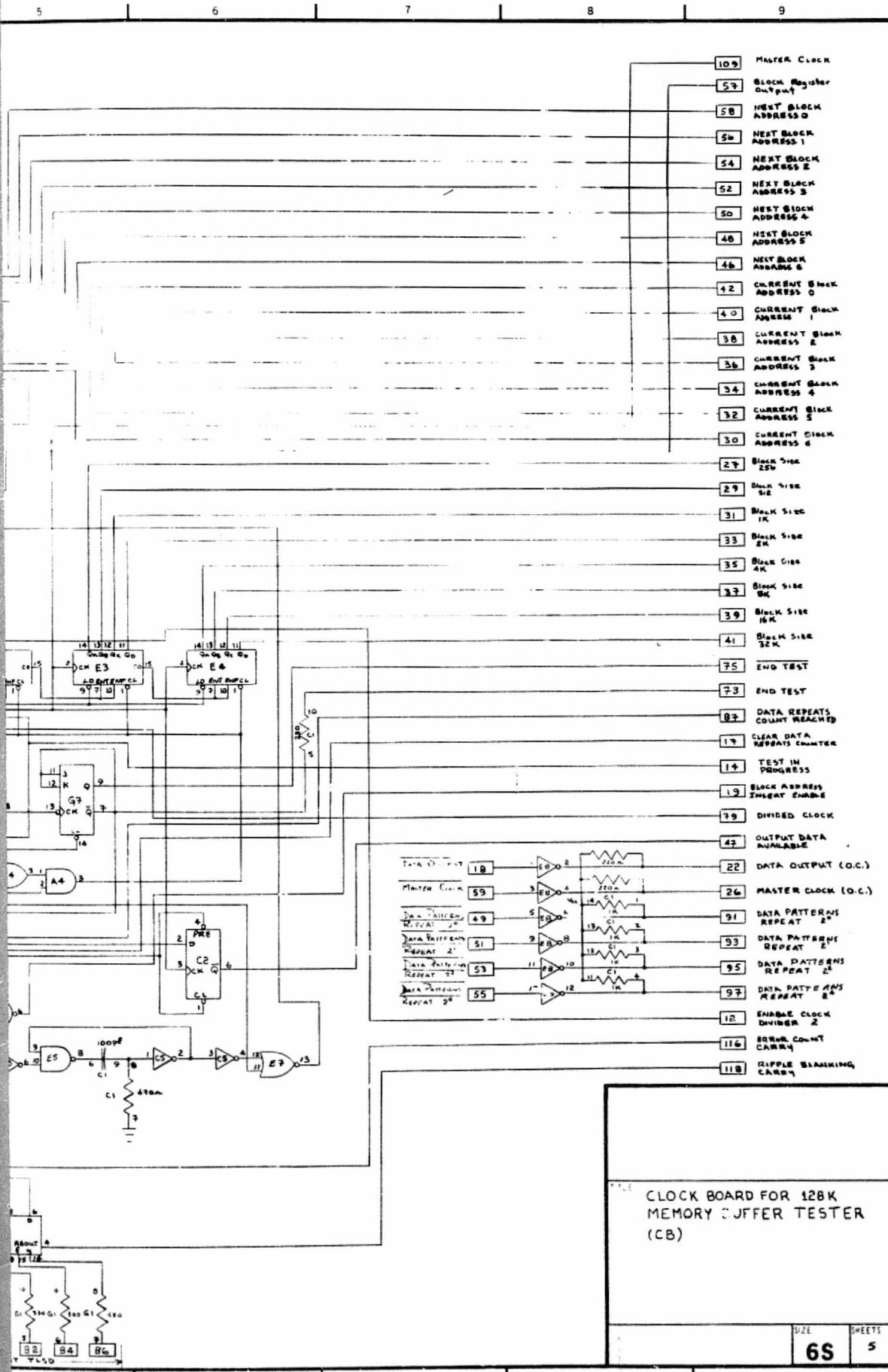
A P P E N D I X F

Memory System Exerciser Schematics



DRAWING NUMBER
TS 3502
1

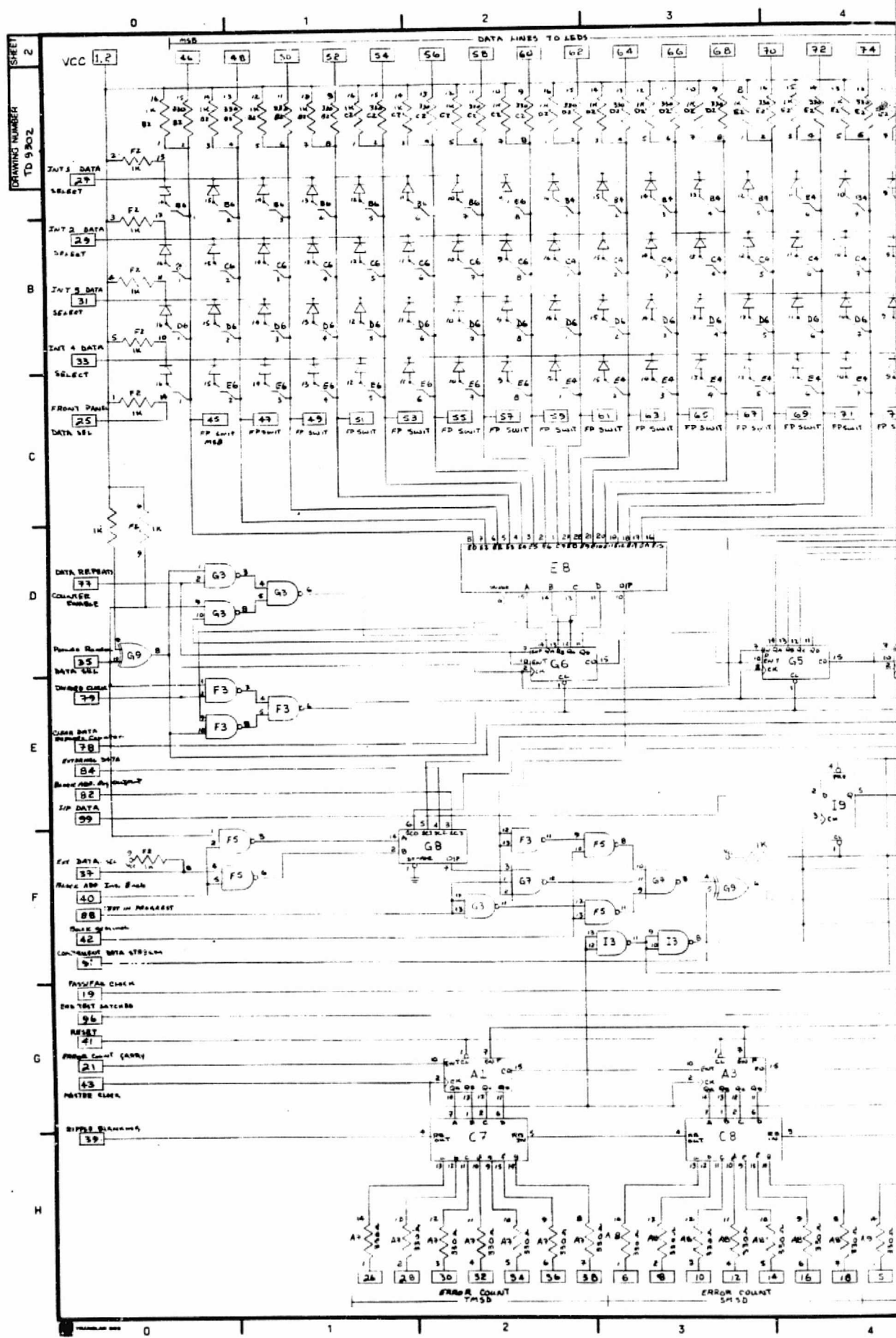
FOLDOUT FRAME

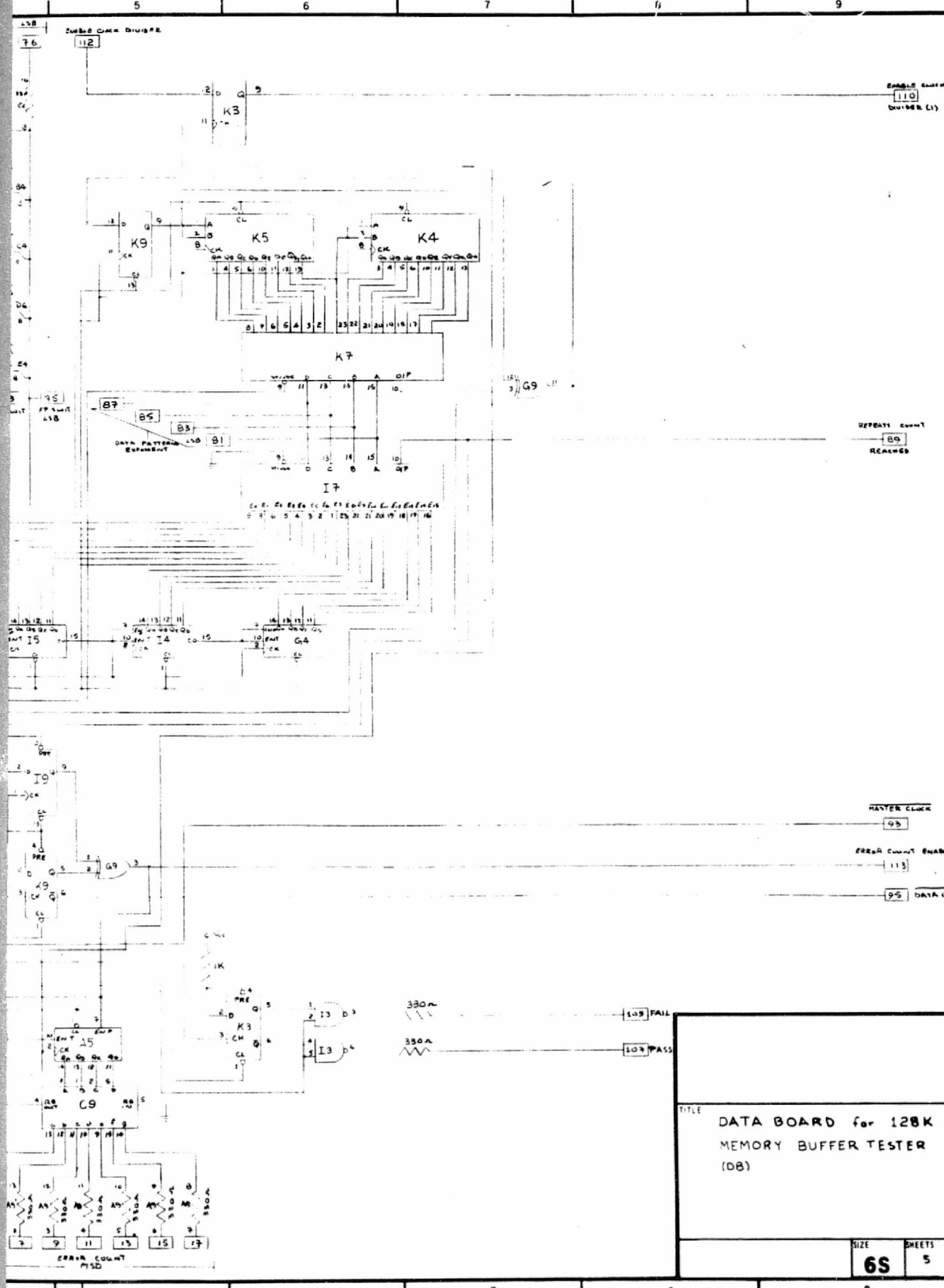


DRAWING NUMBER TD9302	
DATE OCTOBER 30, 1975	
ISSUE 3	AUTHORIZATION BNR RWI
DEVICE LAYOUT	
A1	ADAPTOR
A2	SN74LS153
A3	SN74161
A4	SN74LS08
A5	SN7404
A6	SN74LS74
A7	SN74LS10
A8	SN74LS00
A9	SN74LS157
C1	RESISTOR
C2	SN74LS74
C3	SN74161
C4	SN74LS08
C5	SN74LS04
C6	SN74LS10
C7	SN74LS74
C8	SN74LS74
C9	SN74LS157
E1	RESISTOR
E2	RESISTOR
E3	SN74161
E4	SN74161
E5	SN74LS00
E6	SN74LS00
E7	SN74LS08
E8	SN7404
E9	SN74LS04
G1	RESISTOR
G2	SN7447
G3	SN74184
G4	9.6MHZ CRYSTAL
G5	SN74174
G6	SN74163
G7	SN74LS112
G8	SN74LS153
G9	SN74LS153
I1	SN7447
I2	SN7447
I3	SN74184
I4	SN74LS124
I5	SN74163
I6	SN74163
I7	SN74LS04
I8	SN74LS153
I9	SN74LS112
K1	SN74162
K2	SN74162
K3	SN74162
K4	SN74163
K6	SN74150
K8	SN74123
K9	SN74LS00
A-----K L M N O P Q R S T U V W X Y Z AA AB AC AD AE AF AG AH AI AJ AK AL AM AN AO AP AQ AR AS AT AU AV AW AX AY AZ BA BB BC BD BE BF BG BH BI BJ BK BL BM BN BO BP BQ BR BS BT BU BV BW BX BY BZ CA CB CC CD CE CF CG CH CI CJ CK CL CM CN CO CP CQ CR CS CT CU CV CW CX CY CZ DA DB DC DD DE DF DG DH DI DJ DK DL DM DN DO DP DQ DR DS DT DU DV DW DX DY DZ EA EB EC ED EE EF EG EH EI EJ EK EL EM EN EO EP EQ ER ES ET EU EV EW EX EY EZ FA FB FC FD FE FF FG FH FI FJ FK FL FM FN FO FP FQ FR FS FT FU FV FW FX FY FZ GA GB GC GD GE GF GG GH GI GJ GK GL GM GN GO GP GQ GR GS GT GU GV GW GX GY GZ HA HB HC HD HE HF HG HH HI HJ HK HL HM HN HO HP HQ HR HS HT HU HV HW HX HY HZ IA IB IC ID IE IF IG IH II IJ IK IL IM IN IO IP IQ IR IS IT IU IV IW IX IY IZ JA JB JC JD JE JF JG JH JI JJ JK JL JM JN JO JP JQ JR JS JT JU JV JW JX JY JZ KA KB KC KD KE KF KG KH KI KJ KK KL KM KN KO KP KQ KR KS KT KU KV KW KX KY KZ LA LB LC LD LE LF LG LH LI LJ LK LL LM LN LO LP LQ LR LS LT LU LV LW LX LY LZ MA MB MC MD ME MF MG MH MI MJ MK ML MN MO MP MQ MR MS MT MU MV MW MX MY MZ NA NB NC ND NE NF NG NH NI NJ NK NL NM NO NP NQ NR NS NT NU NV NW NX NY NZ OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP OQ OR OS OT OU OV OW OX OY OZ PA PB PC PD PE PF PG PH PI PJ PK PL PM PN PO PP PQ PR PS PT PU PV PW PX PY PZ QA QB QC QD QE QF QG QH QI QJ QK QL QM QN QO QP QQ QR QS QT QU QV QW QX QY QZ RA RB RC RD RE RF RG RH RI RJ RK RL RM RN RO RP RQ RR RS RT RU RV RW RX RY RZ SA SB SC SD SE SF SG SH SI SJ SK SL SM SN SO SP SQ SR SS ST SU SV SW SX SY SZ TA TB TC TD TE TF TG TH TI TJ TK TL TM TN TO TP TQ TR TS TT TU TV TW TX TY TZ UA UB UC UD UE UF UG UH UI UJ UK UL UM UN UO UP UQ UR US UT UU UV UW UX UY UZ VA VB VC VD VE VF VG VH VI VJ VK VL VM VN VO VP VQ VR VS VT VU VV VW VX VY VZ WA WB WC WD WE WF WG WH WI WJ WK WL WM WN WO WP WQ WR WS WT WU WV WW WX WY WZ XA XB XC XD XE XF XG XH XI XJ XK XL XM XN XO XP XQ XR XS XT XU XV XW XX XY XZ YA YB YC YD YE YF YG YH YI YJ YK YL YM YN YO YP YQ YR YS YT YU YV YW YX YY YZ ZA ZB ZC ZD ZE ZF ZG ZH ZI ZJ ZK ZL ZM ZN ZO ZP ZQ ZR ZS ZT ZU ZV ZW ZX ZY ZZ	
DESIGN AUTHORITY Bell - Northern Research	
RATING	
DRAWING NUMBER TD9302	
SIZE 6S	SHEETS 5
SHEET F-1	

CLOCK BOARD FOR 128K
MEMORY BUFFER TESTER
(CB)

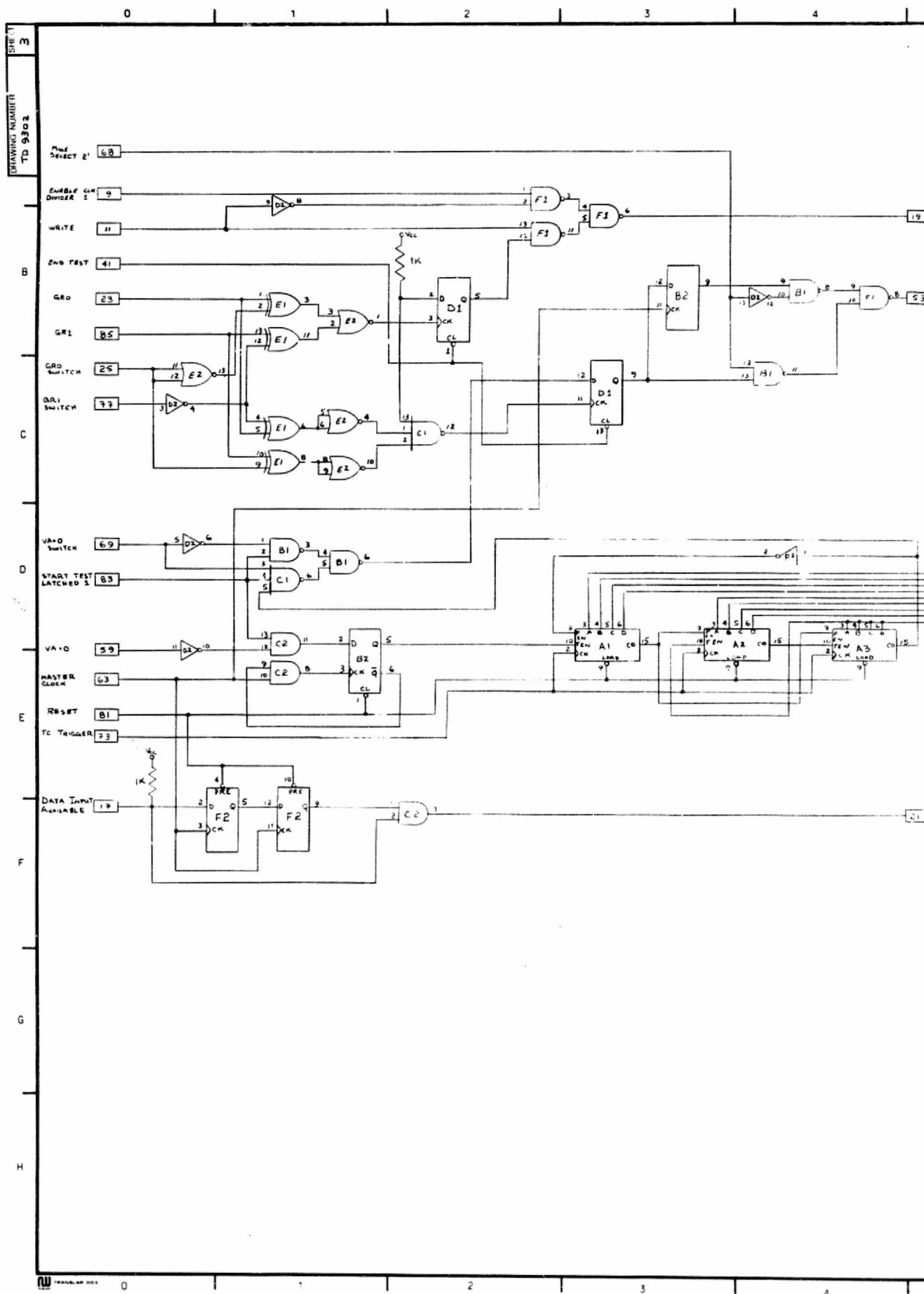
FOLDOUT FRAME





DRAWING NUMBER TD 9302	
DATE Dec 15, 1975	
ISSUE 3	AUTHORIZATION BWR
DEVICE LAYOUT	
A1 - SN74162 A3 - SN74162 A5 - SN74162 A7 - Resistors A9 - Resistors B2 - Resistors B4 - Switches B6 - Switches C2 - Resistors C4 - Switches C6 - Switches C8 - SN74162 C9 - SN74162 D2 - Resistors D4 - Switches D6 - Switches E2 - Resistors E4 - Switches E6 - Switches E8 - SN74150 F2 - Resistors F3 - SN74150 F5 - SN74150 G3 - SN74150 G4 - SN74161 G5 - SN74161 G6 - SN74161 G7 - SN74161 G8 - SN74153 G9 - SN74161 H3 - SN74150 H4 - SN74161 H5 - SN74161 H7 - SN74150 H9 - SN74161 K3 - SN74153 K4 - SN74153 K5 - SN74153 K9 - SN74153	
REPEATS COUNT REACHED	
MASTER CLOCK ERROR COUNT ENABLE DATA OUT	
TITLE DATA BOARD for 128K MEMORY BUFFER TESTER (DB)	
DESIGN AUTHORITY Bell - Northern Research	
RATING	
DRAWING NUMBER TD 9302	
SIZE 6S	SHEETS 5
SHEET F-2	

FOLDOUT FRAME





0100

9

8

7

6

5



F-3

5

69

TD 9302

H

VIRTUAL ADDRESS BOARD
FOR 128K BUFFER MEMORY
SYSTEM TESTER
(VAB)

DESIGN AUTHORITY

FIELD CONNECTOR



D

C

B

A

- A - SN74161
- A2 - SN74161
- A3 - SN74161
- A4 - CTS DIP SWITCH
- B1 - SN74150
- B2 - SN74150
- B3 - DECKMAN 1M2
- C1 - SN74150
- C2 - SN74150
- D1 - SN74150
- D2 - SN74150
- E1 - SN74150
- E2 - SN74150
- F1 - SN74150
- F2 - SN74150

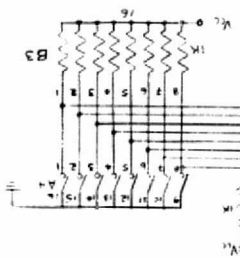
DEVICE LAYOUT

3
REV

DATE
DEC 15/75

TD 9302

DRAWING NUMBER



ENABLE TEST

ENABLE CLOCK

2

DATA
BOARD
(DB)



VIRTUAL
ADDRESS
BOARD
(VAB)

Vec	1	Vec
2	3	
4	5	
6	7	
8	9	
10	11	ENABLE CLOCK DIVIDER 3 (L3B110)
12	13	WRITE (L3B1)
14	15	
16	17	DATA INPUT AVAILABLE (L3B4)
18	19	ENABLE CLOCK DIVIDER 4 (L3B)
20	21	DATA INPUT AVAILABLE 2 (L3B11)
22	23	GRO (VAB 8)
24	25	GRO (VAB 9)
26	27	GRO (VAB 10)
28	29	END TEST (L3B73)
30	31	
32	33	
34	35	
36	37	
38	39	
40	41	
42	43	
44	45	
46	47	
48	49	
50	51	START TEST LATCHED (L3B5)
52	53	
54	55	
56	57	
58	59	VAB (VAB)
60	61	
62	63	MASTER CLOCK (L3B109)
64	65	
66	67	
68	69	VA C SWIT (L3B)
70	71	
72	73	TC TRIGGER (VAB)
74	75	
76	77	GRI SWIT (L3B)
78	79	
80	81	RESET (L3B23)
82	83	START TEST LATCHED 1 (L3B)
84	85	GRI (VAB 9)
86	87	
88	89	
90	91	
92	93	
94	95	
96	97	
98	99	
100	101	
102	103	
104	105	
106	107	
108	109	
110	111	
112	113	
114	115	
116	117	
118	119	GND

(L3B1) MUX 1-12

(L3B1)

(L3B1)

(L3B1)

70 GRI (VAB 85)
71 GRO (VAB 25)
72 GRI
73 GRO

VAB

DRAWING NUMBER
TD9302

DATE
February 6, 1976

ISSUE
3
AUTHORIZATION
RW

NOTE WIRING SIDE
VIEW

A

B

C

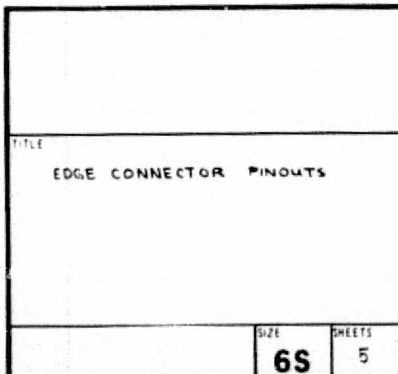
D

E

F

G

H



TITLE
EDGE CONNECTOR PINOUTS

DESIGN AUTHORITY
Bell-Northern Research

RATING

DRAWING NUMBER
TD9302

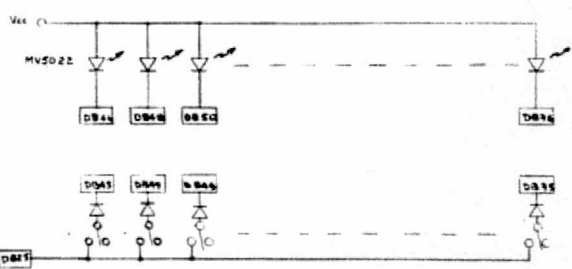
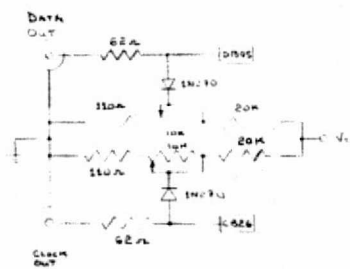
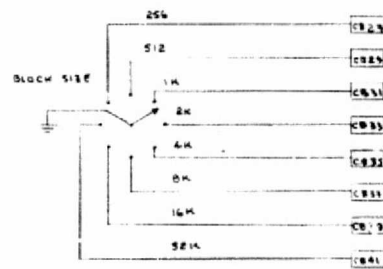
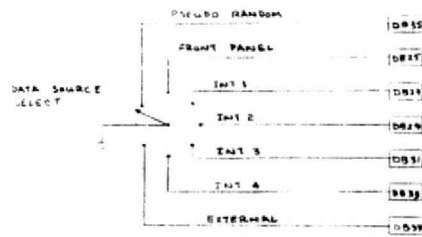
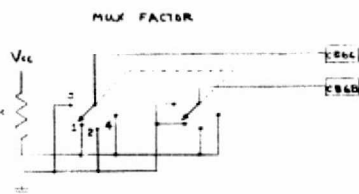
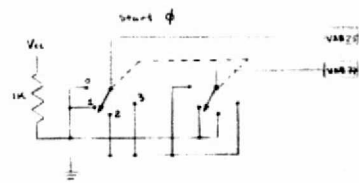
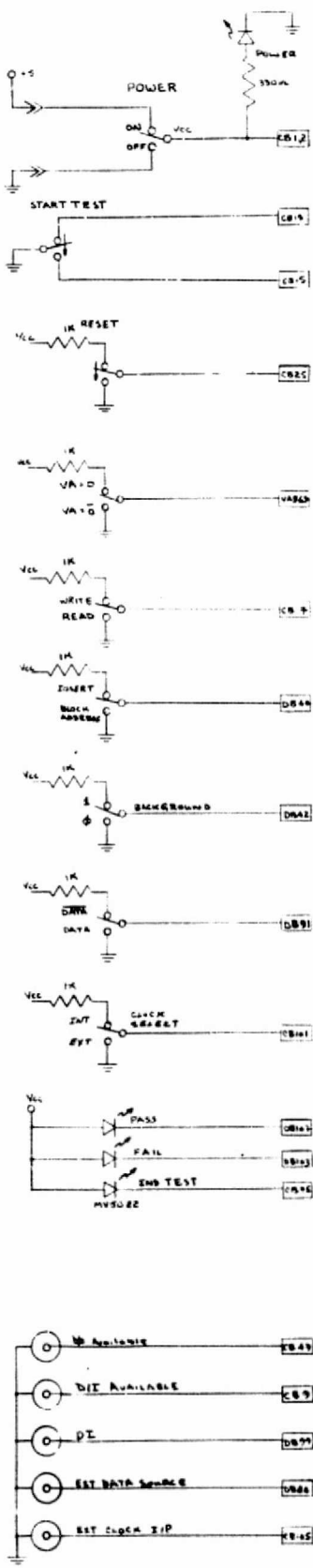
SIZE
6S
SHEETS
5
SHEET
F-4

D100



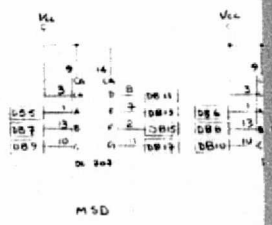
DRAWING NUMBER
TD 9902

SHEET 5
B
C
D
E
F
G
H

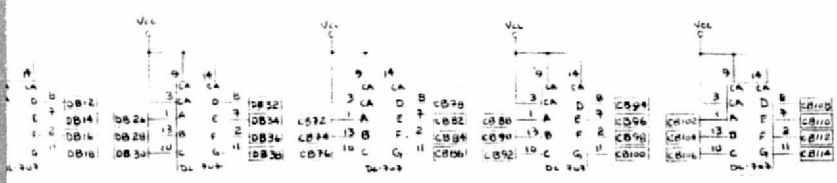
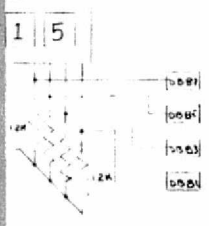
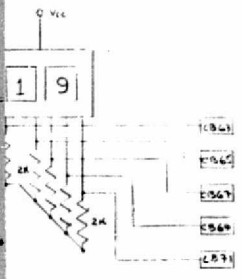


CLOCK FREQ
DIVIDE n
EXPONENT

DATA PATTERNS
REPEATS
EXPONENT






2.



ERROR COUNT

-SD

DRAWING NUMBER TD 9302	
DATE DEC 17/75	
ISSUE 3	AUTHORIZATION BWR NE
NOTE ALL LEFT ARE MVS082	
<div style="text-align: center;">DESIGN AUTHORITY</div> Bell - Northern Research	
RATING	
DRAWING NUMBER TD 9302	
SHEET F-5	 
D100 	

TITLE	
FRONT PANEL WIRING FOR 138K BUFFER MEMORY TESTER	
SIZE	SHEETS
6S	5

APPENDIX G

A 16,384 bit High Density CCD Memory

A 16 384-Bit High-Density CCD Memory

STANLEY D. ROSENBAUM, CHONG HON CHAN, STUDENT MEMBER, IEEE,
J. TERRY CAVES, STEWART C. POON, AND ROBERT W. WALLACE

Abstract—A 16 384-bit charge-coupled device (CCD) memory has been developed for mass storage memory system application where moderate latency, high data rate and low system cost are required. The chip measures only $3.45 \times 4.29 \text{ mm}^2$ ($136 \times 169 \text{ mil}^2$), fits a standard 16-pin package, and is organized as four separate shift registers of 4096 bits, each with its own data input and data output terminals. A two-level polysilicon gate n-channel process was used for device fabrication. A condensed serial-parallel-serial (CSPS) structure was found to provide the highest packing density. Only two external clocks are required driving capacitances of 60 pF each at one-half the data transfer rate. Operations at data rates of 100 kHz to 10 MHz have been demonstrated experimentally, the on-chip power dissipation at 10 MHz being less than 20 $\mu\text{W/bit}$.

I. INTRODUCTION

THE development of the 16-kbit CCD memory to be described here was aimed at filling the gap between the short access time of random-access memories (RAM's) and the longer access time of fixed-head disks with a cost-effective alternative. For the present device, a fourfold system cost advantage over RAM systems is projected. This, however, requires the acceptance of longer access times than those already achieved on CCD's, including block-addressable memories [1], [2] and line-addressable memories [3]. These designs provide access to relatively small blocks of serial data: 256, 256, and 128 bits, respectively, while differing in maximum data rates, operating power, and system overheads for clocking, data transfer and data refreshing. The new 16-kbit

device described here achieves a higher packing density by using an improved form of serial-parallel-serial organization using relatively large arrays of 2048 bits each, two such arrays being paralleled for each block of 4096 bits. Despite this large block size, the worst case access time is only 410 μs , because the device is capable of operating at a data transfer rate of 10 MHz. However, this organization requires a larger number of clock waveforms, which therefore must be generated on-chip in order to minimize the number of external connections and to keep the system overheads low.

II. ORGANIZATION OF CCD ARRAYS FOR HIGH-DENSITY STORAGE

For any given set of geometrical layout rules, serial-parallel-serial (SPS) organizations offer high packing density because only one sense amplifier is required for a large array, such as the 2048-bit array chosen for the present design. This allows space for designing the sense amplifier to detect extremely small amounts of charge, and the CCD storage electrodes can be small, both for this reason and because the electrode dimensions are not limited by any need to pack the sense amplifier into the repeat spacing of every one or two parallel rows. The simplest form of SPS structure is shown in Fig. 1(a). Whenever the M -bit serial input register becomes filled with data, a serial-parallel transfer is made into the first stores of all the M parallel registers, and a parallel-serial transfer into the serial output register occurs whenever this register becomes empty. In the following discussion, it is assumed that these transfers can be made rapidly enough so that the serial data stream need not be interrupted. If there are N bits in every parallel register, and if the input and output dumps are made simultaneously (which is not essential), the total number of bits stored is $M(N + 1)$. However, it is unnecessary to provide

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The authors are with Bell-Northern Research Limited, Ottawa, Ont., Canada.

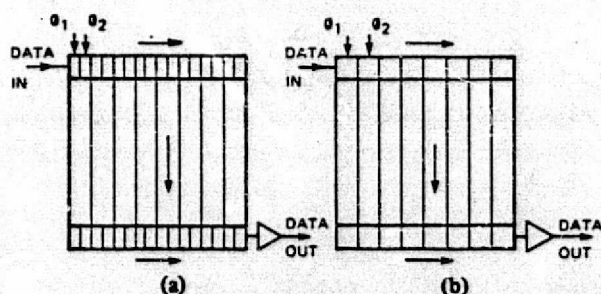


Fig. 1. Schematic diagram of the SPS structures for two-phase CCD's. (a) Standard. (b) Interlaced.

storage for as many as M bits in each of the serial registers; for example, a two-phase register contains two stores per bit, so that an $M/2$ -bit register contains one store for every parallel register. An *interlaced* structure as shown in Fig. 1(b), having input and output serial registers of only $M/2$ bits each, permits a significantly smaller repeat spacing of the parallel registers, which otherwise would be limited by that of the serial registers. The first storage locations of all the parallel registers can then be loaded with data by two successive dumps from the input register, one dump being made from the ϕ_1 stores, and the second dump being made from the ϕ_2 stores after the input register has been refilled. A corresponding procedure can be followed for the output dumps.

After minimizing the repeat spacing of the parallel registers, the next step in achieving highest packing density (again for a given set of layout rules) is to minimize the repeat spacing along the parallel registers. A two-phase structure requires two storage locations per bit, but the density can be increased by almost a factor of two by using the "electrode-per-bit" (E/B) organization, in which a serial string of n bits can occupy adjacent storage locations [4]. The bits are transferred one at a time in sequence, making use of an extra, vacant location which therefore "travels" in the opposite direction to that of transfer. The relative area per bit is then represented by a factor $(n+1)/n$, compared to a factor 2 for ordinary two-phase using the same layout geometries. The $n+1$ storage electrodes require individually timed clock waveforms or "ripple clocks," each of which must have fast edges, because the individual transfers must take place one at a time, within a fraction $1/(n+1)$ of the transfer period for the complete string. Each of the $n+1$ transfer electrodes may be driven from the same clock as is applied to the following adjacent storage electrode, as is done in ordinary two-phase clocking. In practice, the charge-handling capability can be approximately doubled by using separate clocking of the transfer electrodes, making a total of $2(n+1)$ clocks, because this enables the use of "full-bucket" charge storage and transfer, increasing the amount of charge reaching the sense amplifier, with resulting increase in noise margins.

Because of the need for a high net rate of data transfer, the ripple clock organization is best suited to a structure with parallel-multiplexed paths, where the parallel transfer rate is only a fraction $1/M$ of the incoming data rate. This has been called the "multiplexed electrode-per-bit" organization (ME/B) [4] and is particularly well-suited to being adapted to the SPS type of multiplexed structure. However, another problem is

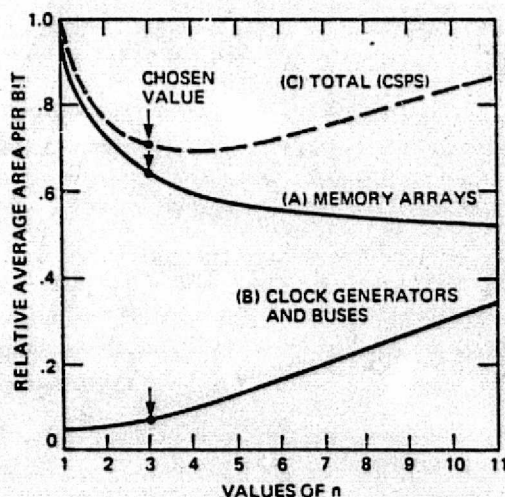


Fig. 2. Relative area per bit versus the number of adjacent bits in a string n .

the difficulty of providing a sequence of $n+1$ clocks on successive locations. It could be done by routing a single high-speed clock to each location in turn by using a decoder or ring-counter circuit, but the geometrical layout of this circuitry may actually require a larger repeat spacing than the CCD electrodes. This "pitch limitation" problem is comparable to that which limits the packing density in RAM's. The difficulty can be avoided by adapting the ripple clock principle to short data strings, requiring only a small number of clock waveforms which can be distributed along buses. The clock waveforms also become easier to generate, because more time is available for each individual transfer, and therefore fast edges are not required. Although the packing density factor $(n+1)/n$ is less favorable when a small value of n is chosen, this disadvantage is more than outweighed by the advantage of being able to retain the same closely packed electrode structure as for ordinary two-phase clocking. As Fig. 2 illustrates, the area advantage obtained by increasing the value of n is relatively small for values of n greater than three, while the area occupied by clock drivers and distribution buses increases linearly with n . The total area reaches a minimum for quite small values of n , the actual position of the minimum depending in a complicated way on geometrical layout considerations. The dotted curve showing total area in Fig. 2 has been drawn by hindsight, using area parameters obtained on the 16 kbit chip, and extrapolated to other values of n .

The combination of an interlaced serial-parallel-serial organization with a ripple-clock scheme characterized by small values of n provides a high density of storage, and will be referred to here as "condensed serial-parallel-serial" or CSPS organization. The factor $n+1$ will be referred to as the ripple spacing.

The choice of CSPS as the optimum organization for CCD memories is only justified if the array size is sufficiently large, otherwise the area occupied by the serial registers and sense amplifiers, and the power they consume, become disproportionately large. Fig. 3 illustrates the relationship between array size and average area per bit, for CSPS arrays having the same ripple spacing and multiplexing factors, cell dimensions, sense amplifier, and input and output buffers as used in the 16-kbit CCD. The averaging takes into account the areas oc-

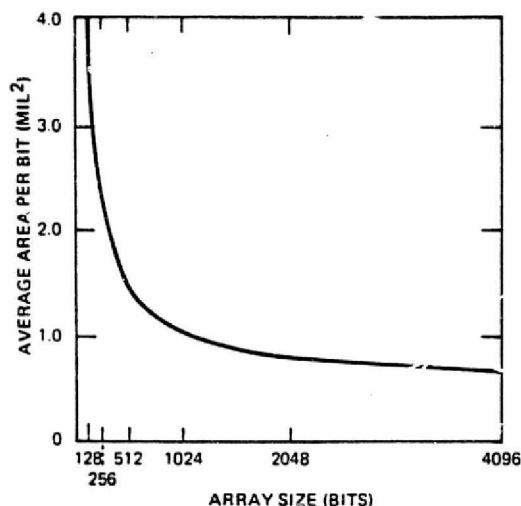


Fig. 3. Average area per bit versus the array size for CSPA structures with $M = 32$ and $n = 3$.

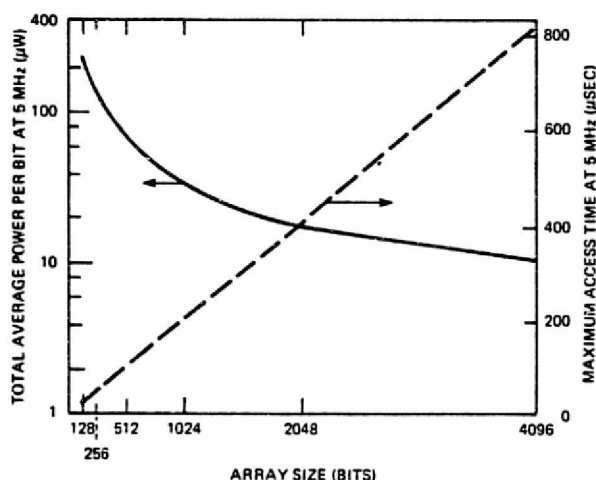


Fig. 4. Average power consumption and maximum access time as a function of array size for CSPA structures with $M = 32$ and $n = 3$.

occupied by the above circuit features, but does not include the area occupied by the clock drivers, clock distribution buses, and other support circuitry, since these facilities can be shared by a number of arrays and therefore do not greatly influence the choice of size for each individual array. Fig. 4 illustrates the corresponding effect of array size on average power consumption per bit. Once again, the contribution made by the shared support circuitry is not included. It may be seen that the CPS organization is more favorable for larger arrays, containing at least 1 kbit each.

III. OPTIMIZATION OF MEMORY CHIP

Considerations such as those illustrated in Figs. 2, 3, and 4 led to the selection of a CSPA organization having the particular value $n = 3$ for the number of adjacent bits in each string, taking into account the area efficiency factor $(n+1)/n$, and the need to avoid undue complexity and area in the clock generator circuitry and clock distribution buses. In the geometrical layout which was chosen, the area of each storage location is $278 \mu\text{m}^2$ (0.43 mil^2), including the area of the associated transfer gate and isolation between adjacent parallel

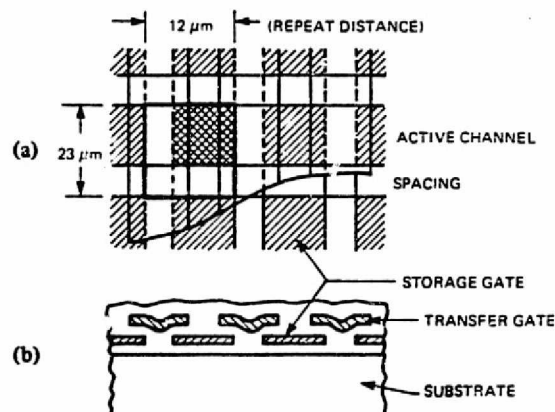


Fig. 5. Layout of the storage and transfer electrodes in the parallel array of the CSPA structure. (a) Plan view. (b) Cross section.

rows, as illustrated in Fig. 5. Allowing for the factor $(n+1)/n = 4/3$, the effective area occupied by each bit stored in the parallel part of the array is $368 \mu\text{m}^2$ (0.57 mil^2). In order to increase the charge-handling capability of the array, and so to broaden the operating margins at the sense amplifier, the option previously discussed of clocking the storage and transfer electrodes with different waveforms was adopted. This required the generation of eight clocks, rather than four for the main parallel array. A multiplexing factor $M = 32$ was chosen, providing 32 parallel registers for each array. Since two arrays are paralleled to make up each block, the effective multiplexing factor is 64 relative to the external data stream, so that at a data rate of 10 MHz the parallel clock frequency is only 156 kHz. Providing two paralleled arrays is considerably more favorable than providing a single array with 64 parallel paths and the same overall block size, since the number of serial transfers experienced by each bit is halved, and the serial transfer frequency is also halved. An array size of 2048 bits was chosen, providing an average area per bit of $419 \mu\text{m}^2$ (0.65 mil^2) for each CCD array, equivalent to $516 \mu\text{m}^2$ (0.8 mil^2)/bit when the array support circuitry is included, as assumed in Fig. 3. Only a small advantage in area per bit and power per bit would have been achieved by choosing a larger array size than 2048 bits, while the access time would have lengthened in proportion. However, another reason for this choice was that it led to a quad-4-kbit configuration on the 16-kbit chip, which was convenient since a standard 16-pin package provides enough pins to permit individual input and output connections to each block, in addition to those required for the dc power rails, two external clocks, and two control inputs.

A third consideration was associated with leakage currents and the corresponding maximum refresh time of a CCD. Since present-day 4-kbit dynamic MOS RAM's are being manufactured to meet a specified refresh time of 2 ms at temperatures up to 70°C , the same considerations apply to CCD's, because the leakage currents have the same physical cause. A refresh time of 2 ms would indicate a minimum working data rate of 2 MHz, which is far enough removed from the maximum of 10 MHz to provide a flexible speed range. In practice a lower data rate than 2 MHz should be practicable, because the maximum storage time is determined

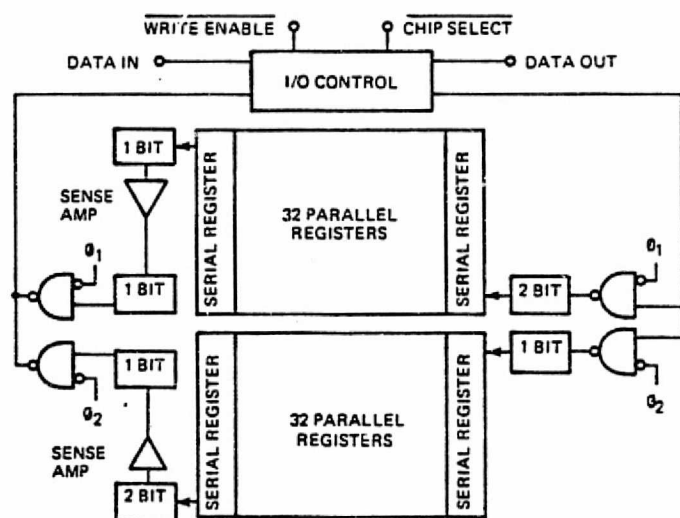


Fig. 6. Block diagram of one 4096 bit shift register on the 16-kbit chip.

by the average leakage current of many storage locations, rather than being limited by the highest leakage location, as in the case of RAM's.

The use of a CSPS structure greatly reduces the undesirable effects of transfer inefficiency, compared to a conventional SPS structure storing the same number of bits. Whereas a conventional two-phase SPS array of 2-kbit size and having 32 parallel paths would subject each charge packet to approximately 66 high-speed transfers and approximately 126 low-speed transfers, the corresponding approximate figures for a CSPS array (assuming $n=3$) would be only 34 high-speed transfers and 84 low-speed transfers. The benefits of paralleling two arrays could, of course be obtained in either case. The actual numbers of transfers for each charge packet in the 16-kbit chip are 37 high-speed transfers and 84 low-speed transfers, for the following reasons. In addition to the regular serial shifts and serial-parallel and parallel-serial shifts, there are several extra high-speed transfers. One extra transfer results from a preliminary storage electrode, used for defining the amount of charge launched. Another simplifies the paralleling of the two arrays for every block: an extra storage electrode is placed before one of the two CSPS arrays, while an extra storage electrode is placed after the other array. In this way, the two arrays accept data from the input buffer in opposite phases, while being clocked together by common clock waveforms. Another extra transfer is used in conveying charge from the CSPS array to the input node of the sense amplifier. Preliminary experiments showed that the 2-kbit CSPS array could transmit data at clock rates up to 4 MHz without use of a bias charge and with adequate operating margins. However, to achieve satisfactory margins at 5 MHz clock rate (10 MHz on the 16K chip) a bias charge (fat zero) of between 10 and 30 percent was found to be helpful.

Fig. 6 shows the organization of one 4-kbit block of memory, including the bit delays associated with the extra transfers. Each transfer causes a delay of one data bit, which is one half of the clock period. The extra bit delay which follows each sense amplifier is discussed in the next section. Despite the extra bit delays, and the complication resulting from the

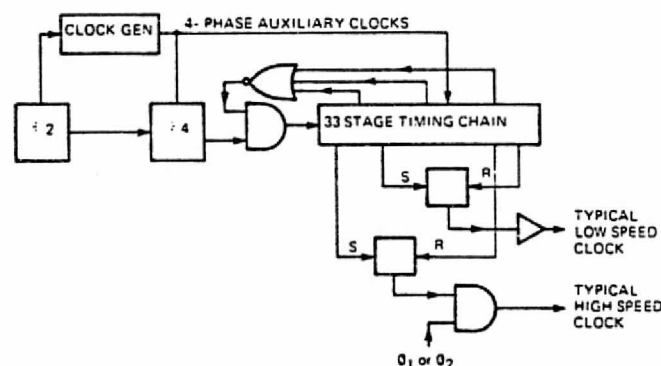


Fig. 7. Block schematic diagram of on-chip clock generation circuitry.

two-phase interlacing of the serial-parallel transfers, the total number of bits stored in the block at any time has been set at 4096 by proper timing of parallel-serial transfers relative to the timing of the serial-parallel transfers.

IV. SUPPORT CIRCUITRY

A block schematic diagram of the on-chip clock generation circuitry is shown in Fig. 7. The external clocks ϕ_1 , ϕ_2 drive a divide-two counter, which in turn generates a set of four-phase clocks for operating the internal circuitry. A divide-4 circuit and feedback logic provide an impulse at the parallel clock rate into a 33-stage timing chain, which in turn provides impulses at the proper times to each of the clock waveform generators. Because of the three feedback tappings on the timing chain, the divide-4 circuit actually functions as a divide-16 counter. Each clock generator can be represented as a set/reset flip-flop, which is set by an impulse from one point on the timing chain, and reset from another point. Those clock generators which operate on the main parallel arrays must drive high capacitances, but are not required to switch at high speed. The clock generators which are associated with transfers into and out of the serial registers drive only small capacitances, but must generate fast edges to synchronize with the serial transfer processes. Therefore, the MOS transistors employed in the output driver of each clock generator are all of comparable size, with channel breadth about 30 times the channel length. These provide more than adequate driving capability for the 16-kbit memory. The counters, timing chain, and clock generators have been designed to clear rapidly any illegal states which might be picked up as a result of external clock irregularities. The circuitry also recognizes a "start-up mode" whenever dc power is applied while both external clocks are low, which does not occur during normal operation. Following recognition of the start up mode, the internal clocks will commence with predictable phases relative to the first turn-on of either of the external clocks, and input data can be supplied within 43 or 45 clock cycles, depending on which external clock turns on first.

The data input buffer was designed to accept the incoming data at TTL levels and to supply the CCD input with the appropriate MOS levels. For a high-level input state, the buffer generates an intermediate voltage level on the CCD input gate to launch a "fat zero" charge of approximately 20-30 percent of a full bucket into the CSPS array. Conversely, for a low

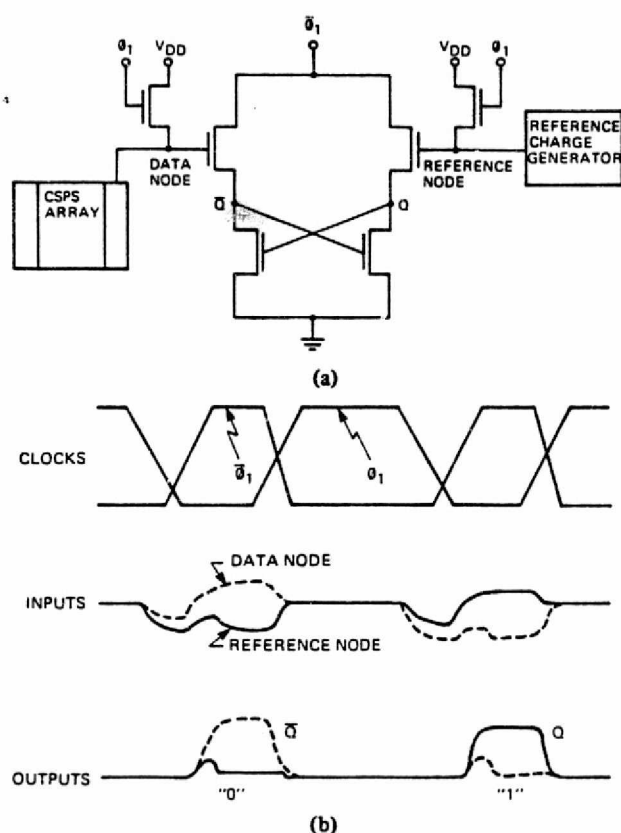


Fig. 8. Sense amplifier for the CSPPS array. (a) Circuit schematic. (b) Clock and signal waveforms (from computer simulation).

level input state a high-level voltage is supplied to the CCD input and a full bucket of charge is launched. Locally generated ϕ_1 and ϕ_2 pulses were used at the CCD inputs to provide two-way data splitting.

The sense amplifier at the output of each 2-kbit array is a differential-input flip-flop, which differs, however, from the sense amplifiers commonly used in MOS RAM's [5], for the following reasons. In the RAM flip-flops, the refresh operation is achieved by positive feedback to the input nodes, one input being raised high, and the other being brought down almost to V_{SS} potential. To bring either input node to V_{SS} would cause errors in the present device, since the node could act as a source, allowing charge to run back into the last storage location of the CCD. This problem is inherent in two-phase CCD's [1]. To avoid this problem, a "load-steered" flip-flop was developed, as shown in Fig. 8, whose operation is as follows. The data node and reference node are precharged high during ϕ_1 clock high level, then ϕ_1 turns off, dumping the data charge packet and the reference charge packet onto their respective nodes. Almost simultaneously, internal clock ϕ_1 turns on, bootstrapping the input nodes to relatively high potentials. Depending on the state of the data, one load element passes more current than the other, and by positive feedback on the driving elements the flip-flop is driven into one of its two states. From computer simulation it was found that for a differential input of 0.5 V the realization time of the flip-flop connected to its load capacitance was approximately 30 ns, limited by the rise time of clock ϕ_1 [Fig. 8(b)]. To achieve such high speed it was necessary to

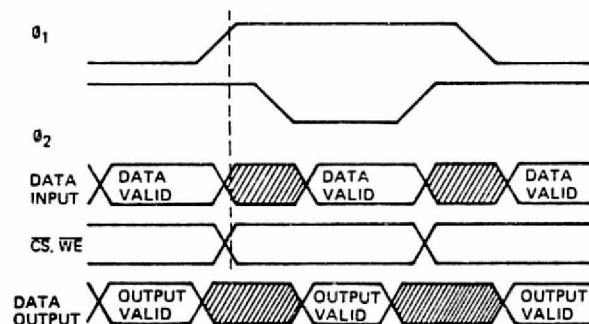


Fig. 9. Operating waveforms and timing diagram of the memory device.

avoid loading the flip-flop with excessive capacitance. This was achieved by using dynamic MOS principles in designing the data output buffer. Functionally, this involved storing the output state of the flip-flop, and driving the output buffer during the following bit time. This also reduced the effective propagation delay between the clock transition and the appearance of valid data at the output terminal to the delay of the output buffer alone, so that the operating frequency was not limited by the output circuitry. The tristate output buffer was designed to drive at least one low power Schottky TTL gate. Individual 2-kbit CSPPS arrays using this sense amplifier and output buffer were successfully operated at a speed of greater than 7 MHz, which would be equivalent to a data rate of 14 MHz on the 16K chip.

Two control inputs, $\overline{\text{CHIP SELECT}}$ ($\overline{\text{CS}}$) and $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$), and associated circuitry were provided, designed for operation up to 10-MHz data rate in three functional modes: RECIRCULATE, ($\overline{\text{CS}}$ high), READ and RECIRCULATE ($\overline{\text{CS}}$ low, $\overline{\text{WE}}$ high), READ and WRITE ($\overline{\text{CS}}$ low, $\overline{\text{WE}}$ low). In READ and WRITE mode, the 4-kbit blocks function as digital delay lines, which may be serially interconnected to form larger blocks with no penalty in maximum data rate. It was considered to be important that $\overline{\text{CHIP SELECT}}$ would operate from ordinary 5-V TTL signals, since these signals must be generated individually for all the memory devices which are OR tied to common data buses. $\overline{\text{WRITE ENABLE}}$ requires a full clock level, but this is not a serious disadvantage because this signal can be supplied to a group of devices from a common driver.

Fig. 9 shows the timing diagram of the operating waveforms of the 16-kbit memory. Only two high level clocks (ϕ_1 , ϕ_2) and a high level $\overline{\text{WE}}$ control input are needed, all data inputs, data outputs and $\overline{\text{CS}}$ control input are TTL levels.

V. CHIP LAYOUT

The timing chain and clock generators which were common to all four memory blocks were distributed along the center axis of the chip, since this was found to minimize the area required by interconnections. The resulting layout is shown in Fig. 10. The four data input buffers were located along the central region also, so that the sense amplifiers, output buffers, and local clock generators could be situated along the two longer sides of the chip. The input/output control circuits were placed along the shorter sides, as were all the bonding pads for external connections, since this provided a rectangular

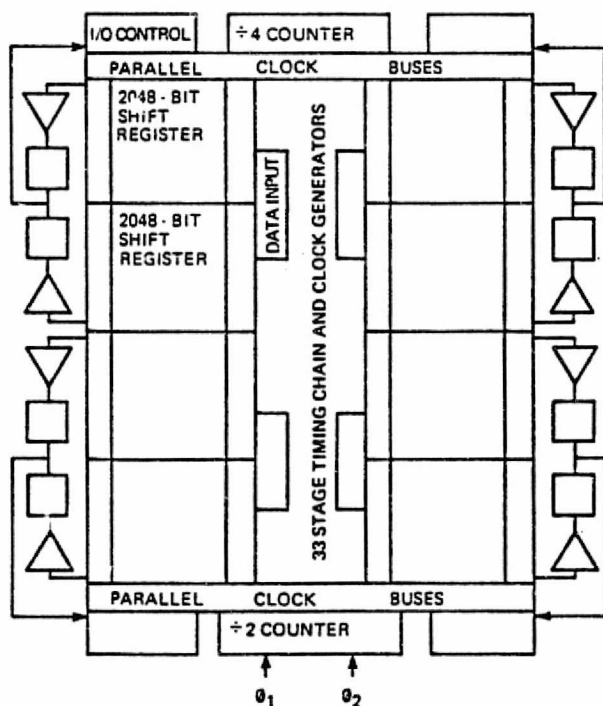


Fig. 10. Chip layout diagram of the 16 384-bit CCD memory.

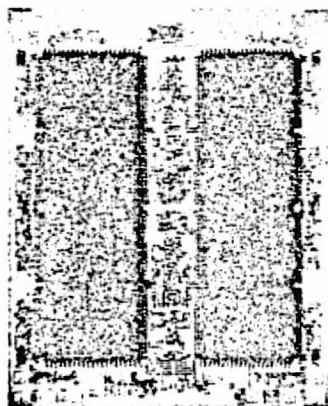


Fig. 11. Photomicrograph of the 16-kbit chip.

chip format which was more economical in total area, and also more suited to being fitted into a standard 16-pin dual-in-line package. The overall dimensions of the chip are 3.45 mm (136 mils) by 4.29 mm (169 mils), the average area per bit of storage being $900 \mu\text{m}^2$ (1.4 mil^2). Comparing this figure with the $516 \mu\text{m}^2$ (0.8 mil^2)/bit occupied by the CSPS arrays and local support circuits alone, it can be seen that the common circuit overheads increase the area per bit by a considerable amount, although the area per bit is still very attractive compared to MOS 4-kbit RAM's which typically occupy a chip of the same size.

VI. EXPERIMENTAL VERIFICATION

The 16-kbit CCD memory was designed and fabricated using a two-level polysilicon gate n-channel process [6]. A photomicrograph of the finished device is shown in Fig. 11.

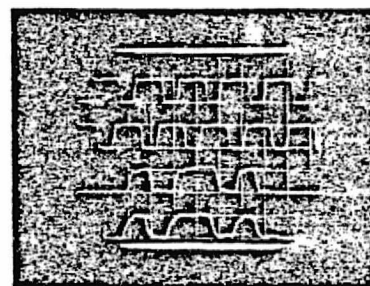
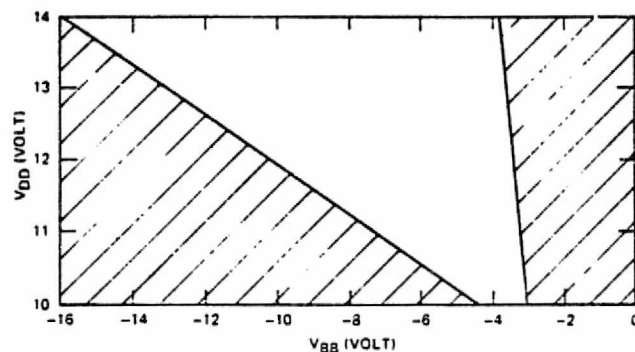
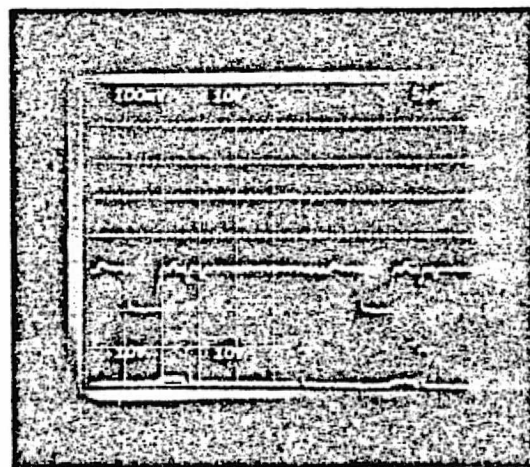
Fig. 12. Typical waveforms of the clocks and data. Top two traces: ϕ_1 and ϕ_2 , 10 V/div. Bottom two traces: data input and data output, 5 V/div. Time scale: 200 ns/div.

Fig. 13. Typical operating range of the supply voltages at a data rate of 10 MHz.

Fig. 14. Clock waveforms as observed on 16-kbit chip. Top two traces: external clocks ϕ_1 and ϕ_2 . Bottom two traces: examples of internally-generated clocks: upper trace shows one of the four low speed clocks which drive the storage electrodes of the parallel array; lower trace shows the high speed serial-parallel strobe pulse. All traces 10 V/div, 5 μs /div.

For most purposes of testing for data throughput, the input data were set up to fill the parallel arrays with diagonal patterns of isolated ONE's in a background of ZERO's, and then inverted to replace this by a pattern of isolated ZERO's in a background of ONE's. These patterns were generated by setting a ONE in

a background of ZERO's, repeating the ONE every 66 bits for a total of 4096 bits, and then generating the complementary sequence for another 4096 bits. The output data were verified by comparison with a repeat of the input test data.

It was found that these patterns were effective for most purposes, and especially for measuring the operating margins of the device at high frequencies, because the effects of charge transfer inefficiency are especially pronounced for isolated ONE's or isolated ZERO's. An example of the input and output data waveforms at a data frequency of 10 MHz is shown in Fig. 12. Diagonal test patterns do not show up clearly on the monitoring oscilloscope, and therefore a nondiagonal test pattern was used to make this photograph. Fig. 13 shows an example of the operating range of dc and clock supply voltages, also at a data frequency of 10 MHz. Two examples of the internally-generated clock waveforms are shown in Fig. 14, together with the two external clocks ϕ_1 , ϕ_2 for comparison, the external clock frequency being 5 MHz. One example shows one of the low-speed clocks applied to storage electrodes in the parallel array, running at the parallel transfer frequency of 156 kHz. The uneven amplitude of the clock high level is caused by capacitive coupling with adjacent electrodes, and is not a defect. The second example shows a strobe clock, used to enable the serial-parallel transfers. This clock produces two pulses at the parallel transfer frequency, one pulse having ϕ_1 timing, and the other having ϕ_2 timing, as required for the two-phase interlacing.

The principal contribution to operating power is the current drain from the positive dc supply, (V_{DD} to V_{SS}), and at 10 MHz this amounts to almost 300 mW at a +12 V supply, about 18 μ W per bit. Half of this power is dissipated in the output buffers and sense amplifiers, for high speed sensing and to provide TTL compatible outputs. The other half of the power is dissipated equally among 1) the data input buffers with local clock inverters, 2) the \overline{CS} inverters for I/O control, and 3) the on-chip clock generation circuits. It is evident that a fair proportion of the power is dissipated to achieve TTL compatibility. Notice that only a fraction (1/6) of the total power is needed to generate all the necessary waveforms to drive the CSPS arrays.

A smaller contribution of 60 mW is dissipated in the external clock drivers, resulting in a total operating power of approximately 22 μ W per bit at 10 MHz. By monitoring the transient current drain for the dc power supply, it was verified that the major current drain occurs during $\phi_1 - \phi_2$ clock overlap, and overall drain is therefore reduced greatly by reducing the overlap to between 10 and 20 ns, which is readily achieved using ordinary circuit techniques. At low frequencies the overall drain is reduced, since the clock overlaps occupy a smaller fraction of the total cycle, and the remaining power drain is largely caused by the eight sense amplifiers.

VII. CONCLUSIONS

This work has demonstrated the practical realization of a 16 384-bit CCD memory on a silicon chip which is small enough for high yield, low cost manufacturing by present-day

techniques, and suitable for applications requiring low overall system cost per bit of storage. The result was made possible by the introduction of a condensed serial-parallel-serial organization as a way to achieve optimum packing density, taking into account the practical problems of peripheral pitch limitations, and the need to generate the clock waveforms on-chip by circuitry of small total area. Although many improvements of detail can still be made to the design, to reduce chip size and power drain still further, the device as described should be a suitable candidate for filling the "access gap" in memory technologies. In addition, extension of the CSPS concept to memory chips of at least 64 kbits can be readily predicted, making use of new developments in processing technology which are already being applied to the development of other MOS and CCD structures.

ACKNOWLEDGMENT

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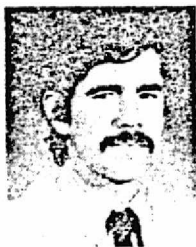
He was a Research and Teaching Assistant in the Department of Electrical Engineering, University of Waterloo, between 1967 and 1973. In 1973 he joined Bell-Northern Research, Ottawa, Ont., Canada as a member of the Scientific Staff, working in the Silicon Technology Laboratory. He is presently engaged in MOS and charge-coupled devices circuit designs, and is working towards the Ph.D. degree at the University of Waterloo.



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development program, concentrating mainly on digital applications and MOS support circuitry.



Robert W. Wallace was born in Calgary, Alta., Canada, on November 7, 1953. He graduated from the Southern Alberta Institute of Technology, Calgary, Alta., Canada, with an honors diploma.

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A P P E N D I X H

Preliminary Specifications of the CC16M1

Recirculating Serial Memory

N-CHANNEL CCD 16K BIT (4096 x 4) RECIRCULATING SERIAL MEMORY CC16M1
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FEATURES

- N-Channel 2-Level Silicon Gate Fabrication
- Organized for Mass Memory (Silicon Disk) Applications
- TTL Compatible Inputs/Outputs
- $\pm 5V$, $+12V$ Power Supplies
- Low Power Dissipation, $<20\mu W/\text{bit}$ at Max. Data Rate
- Two Overlapping Clocks at Half Data Rate
- Clock Capacitances 60pF
- All Other Clocks Generated on-Chip.
- Data Rate from 1 to 10 Megabits/sec.
- Tri-state Outputs
- Separate CHIP SELECT and WRITE ENABLE Inputs
- Configuration - Quad 4096 Bit

DESCRIPTION

The CC16M1 is a 16K bit CCD memory, organized as four shift registers of 4096 bits each with separate inputs and tri-state outputs. Each input data stream is split into two serial-parallel-serial memory arrays of 2048 bits each, providing high-density storage. Data access is controlled by CHIP SELECT (\overline{CS}) and WRITE ENABLE (\overline{WE}) inputs. When \overline{CS} is high, the outputs are held in the off (high impedance) state*. Output data from all four shift registers become available at the output terminals whenever \overline{CS} is held low. Writing into all four shift registers occurs whenever both \overline{CS} and \overline{WE} are turned low; for all other conditions of \overline{CS} and \overline{WE} , data in all four shift registers recirculates automatically. The input or output data terminals or \overline{WE} terminals of different packages may be OR-tied together.

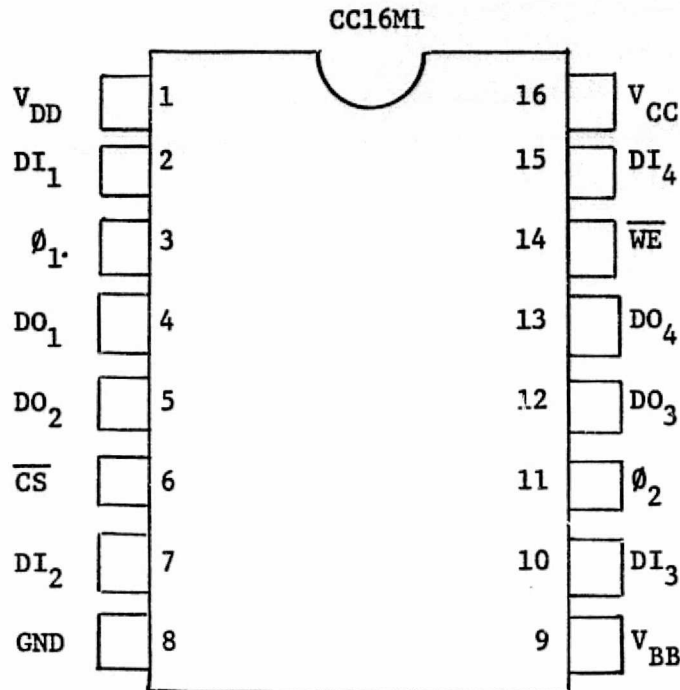
The CC16M1 generates several internal clocks, to operate the memory arrays. Following any interruption of power supplies or clocks, a minimum of 43 clock cycles should be allowed to elapse before any data is written into the device.

* Except during $\phi_1 - \phi_2$ overlap, when DATA OUTPUT = DATA INPUT

PRELIMINARY SPECIFICATIONS

H-2

N-CHANNEL CCD 16K BIT (4096 x 4) RECIRCULATING SERIAL MEMORY CC16M1



PIN CONFIGURATIONS OF CC16M1

PIN NAMES

DI ₁ , DI ₂ , DI ₃ , DI ₄	DATA INPUTS
DO ₁ , DO ₂ , DO ₃ , DO ₄	DATA OUTPUTS
φ ₁ , φ ₂	CCD CLOCK INPUTS
CS	CHIP SELECT INPUT
WE	WRITE ENABLE INPUT
V _{DD} , V _{BB} , V _{CC} , GND	POWER SUPPLIES

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to + 70°C
Storage Temperature	-65°C to + 150°C
Voltages on Any or All Terminals with Respect to V _{BB}	-0.3V to + 25V
Power Dissipation	1.0W

* stresses above the Absolute Maximum Ratings may cause permanent damage to the device.

PRELIMINARY SPECIFICATIONS

H-3

N-CHANNEL CCD 16K BIT (4096 x 4) RECIRCULATING SERIAL MEMORY CC16M1

D.C. OPERATING CHARACTERISTICS

$$T_{\text{ambient}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}, \quad V_{\text{cc}} = +5\text{V} \pm 5\% \quad V_{\text{SS}} = 0\text{V}$$

SYMBOL	PARAMETERS	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
V_{DD}	Power Supply (DC)	11	12	13	V	see operating range chart
V_{BB}	Power Supply (DC)	-6	-5	-4	V	
$V_{\phi\text{H}}$	ϕ_1, ϕ_2 Input High Voltage	$V_{\text{DD}} - 2$	$V_{\text{DD}} - 1.5$	$V_{\text{DD}} - 1$	V	
$V_{\phi\text{L}}$	ϕ_1, ϕ_2 Input Low Voltage	-0.3	0.2	0.8	V	
V_{IH}	Data Input High Voltage	3.0	3.5	$V_{\text{DD}} + 2$	V	
V_{IL}	Data Input Low Voltage	-0.3	0.2	0.8	V	
V_{SH}	$\overline{\text{CS}}$ High Voltage	3.0	3.5	$V_{\text{DD}} + 2$	V	
V_{SL}	$\overline{\text{CS}}$ Low Voltage	-0.3	0.2	0.8	V	
V_{WH}	$\overline{\text{WE}}$ High Voltage	$V_{\text{DD}} - 2$	V_{DD}	$V_{\text{DD}} + 2$	V	
V_{WL}	$\overline{\text{WE}}$ Low Voltage	-0.3	0.2	0.8	V	
V_{OH}	Data Output High Voltage	2.4		V_{CC}	V	$\overline{\text{CS}}$ Low, One LS TTL Load per Output
V_{OL}	Data Output Low Voltage	0	0.2	0.8	V	
I_{DD1}	Standby V_{DD} Supply Current			22	mA	$\overline{\text{CS}}$ High, 10 MHz
I_{DD2}	Average V_{DD} Supply Current			16	mA	$\overline{\text{CS}}$ High, 1 MHz
				27	mA	$\overline{\text{CS}}$ Low, 10 MHz
I_{CC}	Average V_{CC} Supply Current			2.8	mA	$\overline{\text{CS}}$ Low, One LS TTL Load per Output at 10 MHz
I_{BB}	Average V_{BB} Supply Current			100	μA	$V_{\text{BB}} = -5\text{V}, V_{\text{DD}} = +12\text{V}$

PRELIMINARY SPECIFICATIONS

H-4

N-CHANNEL CCD 16K BIT (4096 x 4)
RECIRCULATING SERIAL MEMORY CC16M1

SYMBOL	PARAMETERS	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
$I_{\phi H}$	ϕ_1, ϕ_2 High Current			1.25	mA	
$I_{\phi L}$	ϕ_1, ϕ_2 Low Current			50	μA	
I_{IH}	Data Input High Current			10	μA	
I_{IL}	Data Input Low Current			10	μA	
I_{SH}	\overline{CS} High Current			10	μA	
I_{SL}	\overline{CS} Low Current		2	5*	mA	$V_{\phi H} = V_{DD} = 12V$
I_{WH}	\overline{WE} High Current			10	μA	
I_{WL}	\overline{WE} Low Current			10	μA	
I_{OH}	Output High Current			10	μA	$V_{OH} = V_{CC}, \overline{CS} \text{ Low}$
I_{OL}	Output Low Current	0.4			mA	$V_{OL} = 0.4V, \overline{CS} \text{ Low}$

* Maximum Current Sink occurs during t_o , the Overlap time between ϕ_1 and ϕ_2 .

PRELIMINARY SPECIFICATIONS

H-5

N-CHANNEL CCD 16K BIT (4096 x 4) RECIRCULATING SERIAL MEMORY CC16M1

A.C. CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{SS} = 0V$

SYMBOL	PARAMETERS	LIMITS			UNIT
		MIN.	TYP.	MAX.	
t_H	Clock (ϕ_1, ϕ_2) High Time	120		1000	ns
t_L	Clock (ϕ_1, ϕ_2) Low Time	60		940	ns
t_O	Clocks Overlap Time	20		100	ns
t_{HL}	Clock High to Low Transition Time	10	20	100	ns
t_{LH}	Clock Low to High Transition Time	10	20	100	ns
t_c	Cycle Time	200		2000	ns
t_{si}	Input Setup Time	30			ns
t_{hi}	Input Hold Time	0	15		ns
t_{ss}	\overline{CS} , \overline{WE} Setup Time	15			ns
t_{hs}	\overline{CS} , \overline{WE} Hold Time	0	5		ns
t_d	Output Delay Time			30	ns
t_v	Output Valid Time	30			ns

CAPACITANCES

$T_A = 25^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5 \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	NOMINAL LIMIT	UNIT	CONDITIONS
C_{IN1}	Input Capacitance	6	pF	\overline{CS} Low, \overline{WE} Low
C_{IN2}	Input Capacitance	4	pF	All other Conditions
C_{OUT1}	Output Capacitance	8	pF	\overline{CS} Low
C_{OUT2}	Output Capacitance	3	pF	\overline{CS} High
C_ϕ	Clock (ϕ_1, ϕ_2) Capacitance	60	pF	
$C_{\phi 12}$	ϕ_1 to ϕ_2 Capacitance	8	pF	
C_s	\overline{CS} Capacitance	8	pF	
C_w	\overline{WE} Capacitance	6	pF	

PRELIMINARY SPECIFICATIONS

H-6

N-CHANNEL CCD 16K BIT (4096 x 4)
RECIRCULATING SERIAL MEMORY CC16M1

OPERATING WAVEFORMS

